Mini-Circuits

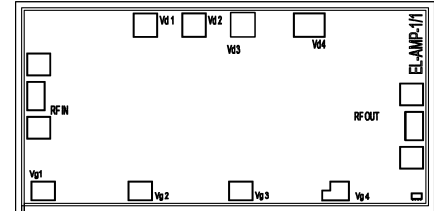
SUPER WIDEBAND, HIGH GAIN, MEDIUM POWER

Monolithic Amplifier Die AVA-20453MP-D+

50Ω 20 to 45 GHz

THE BIG DEAL

- Ultra Wideband, 20 to 45GHz
- Excellent Input and Output Return Loss >10 dB Typ.
- Medium Power, 20dBm typical P1dB.
- Excellent Alternative to AMMC-5040 & TGA4040[a,b]



APPLICATIONS

- 5G
- Point-to-Point Radio
- Military
- Instrumentation

+RoHS Compliant
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

SEE ORDERING INFORMATION ON THE LAST PAGE

PRODUCT OVERVIEW

AVA-20453MP-D+ is a GaAs, pHEMT, MMIC 4-Stage Amplifier Die that operates from 20 to 45 GHz. The amplifier typically provides 23.9 dB Gain and 20 dBm Output Power at 1 dB Gain Compression, 29.4 dBm Output IP3. The amplifier is well-matched to 50 Ohm at both input and output. AVA-20453MP-D+ is a current-biased amplifier that can operate with a single VDD of 4.5V and a single VG that tunes for 300mA operation.

KEY FEATURES

Feature	Advantages
Super-Wide Bandwidth with Flat Gain • 20.4 ±3.5 dB over 20-45GHz	General Purpose Wideband Amplifier is suitable for wide variety of applications.
Medium Output Power • 20dBm Typical P1dB	The combination of High Gain and High Output Power reduces the need for cascading several amplifiers to get the same performance.
High Output IP3 • 29 dBm Typical at Pout = 10dBm/Tone	Easy to integrate into signal chain.
Excellent Wideband In/Out Return Loss • >10 dB from 20 to 45 GHz	
Unpackaged Die	Enables user to integrate it directly into hybrids

A. Suitability for model replacement within a particular system must be determined by and is solely the responsibility of the customer based on, among other things, electrical performance criteria, stimulus conditions, application and compatibility with other components and environmental conditions and stresses.
B. The AMMC-5040 & TGA4040 part number is used for identification and comparison purposes only

REV. OR
ECO-010675
AVA-20453MP-D+
MCLNY
211116

ELECTRICAL SPECIFICATIONS[1] AT 25°C, 50Ω, UNLESS NOTED

Parameter	Condition (GHz)	VDD = 4.5V, IDD = 300mA			Units
		Min.	Typ.	Max.	
Frequency range		20		45	GHz
Gain	20		23.8		dB
	25		23.9		
	30		19.5		
	35		18.6		
	40		16.9		
	45		20.4		
Input Return loss	20		13.1		dB
	25		12.0		
	30		13.7		
	35		16.9		
	40		13.0		
	45		17.3		
Output Return loss	20		15.9		dB
	25		31.8		
	30		15.1		
	35		11.1		
	40		11.5		
	45		10.9		
P1dB	20		19.9		dBm
	25		20.9		
	30		20.1		
	35		19.6		
	40		19.6		
	45		17.7		
OIP3 (Pout= 10 dBm/Tone)	20		30.1		dBm
	25		29.4		
	30		28.2		
	35		27.8		
	40		27.3		
	45		27.0		
Noise Figure	20-45		10.2		dB
Device operating voltage (VDD)		3	4.5	5	V
Device operating current (IDD)			300	350	mA
Device Gate Voltage (VG) , adjusted to IDD = 300mA			-0.45		V
Pinch-off Voltage for VG (Vp), VDD =4.5V, IDD<10mA			-1.5		V
Thermal resistance, junction-to-ground Lead			27		°C/W

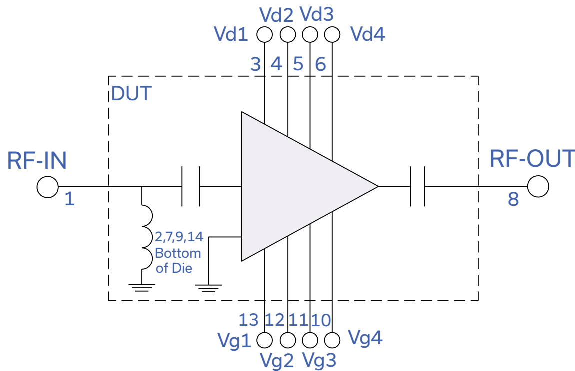
1. Measured on Mini-Circuits Characterization Test Board. See Characterization Test & Application Circuit (Fig. 1)

MAXIMUM RATINGS[2]

Parameter	Ratings
Operating temperature (ground lead)	-40°C to 85°C
Junction Temperature	150°C
Total power dissipation	2W
Input power (CW)	21 dBm
DC voltage at VDD	6V
DC voltage at VG	-3V to +0.5V

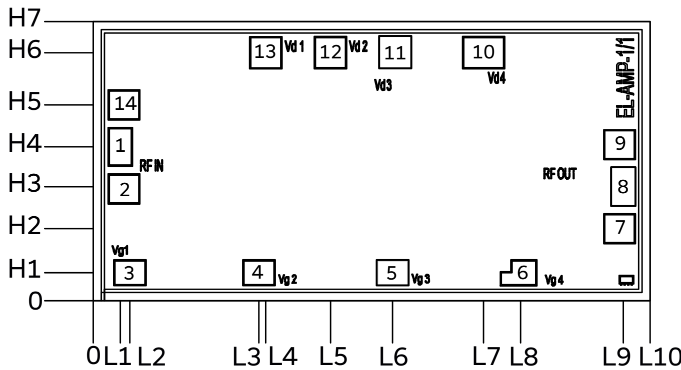
2. Permanent damage may occur if any of those limits are exceeded. Electrical maximum ratings are not intended for continuous normal operation

SIMPLIFIED SCHEMATIC AND PAD DESCRIPTION



Pad #	Function	Description (Refer to Figure 1)
1	RF-IN	RF Input Pad
3	Vd1	Drain Voltage for Stage 1, Connects to VDD via Bypass Cap C1, C9 & C11
4	Vd2	Drain Voltage for Stage 2, Connects to VDD via Bypass Cap C2, C9 & C11
5	Vd3	Drain Voltage for Stage 3, Connects to VDD via Bypass Cap C3, C9 & C11
6	Vd4	Drain Voltage for Stage 4, Connects to VDD via Bypass Cap C4, C9 & C11
8	RF-OUT	RF Output Pad
10	Vg4	Gate Voltage for Stage 4, Connects to VG via Bypass Cap C8, C10 & C12
11	Vg3	Gate Voltage for Stage 3, Connects to VG via Bypass Cap C7, C10 & C12
12	Vg2	Gate Voltage for Stage 2, Connects to VG via Bypass Cap C6, C10 & C12
13	Vg1	Gate Voltage for Stage 1, Connects to VG via Bypass Cap C5, C10 & C12
2,7,9,14 & Bottom of Die	Ground	Connects to Ground

BONDING PAD POSITION



Dimension in um, Typical

L1	L2	L3	L4	L5	L6	L7	L8	L9	L10
84.0	113.0	512.0	533.0	733.0	925.0	1206.0	1321.0	1637.0	1720

H1	H2	H3	H4	H5	H6	H7	Thickness	Die size
86.0	222.0	352.0	476.0	606.0	767.0	863.0	100	1720 x 863

Pad Size 1 & 8	Pad Size 2,7, 9 & 14	Pad Size 3,4 & 5	Pad Size 6	Pad Size 10	Pad Size 11	Pad Size 12 & 13
68 x 113	91 x 86	93 x 73	106 x 73	123 x 93	100 x 100	93 x 93

CHARACTERIZATION, APPLICATION CIRCUIT & ASSEMBLY DRAWING

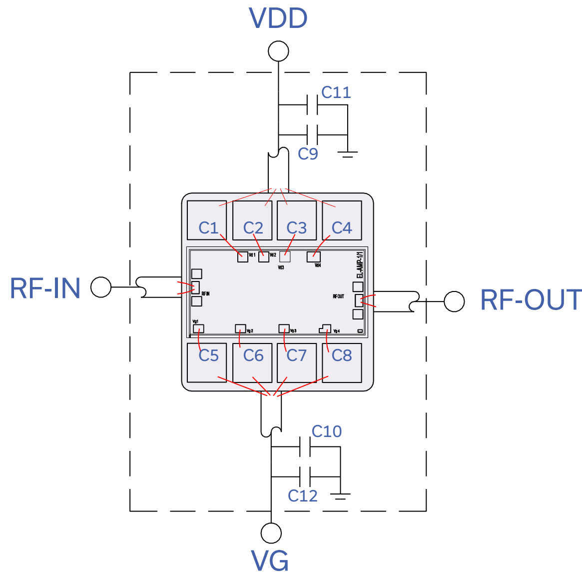


Fig 1. Characterization, Application Circuit & Assembly Drawing
Note: This block diagram is used for characterization. (DUT was soldered on test board of Mini-Circuits Characterization Test Board). Gain, Return loss, Output power at 1 dB compression (P1dB), output IP3 (OIP3) and noise figure measured using Agilent's N5242A PNA-X microwave network analyzer.

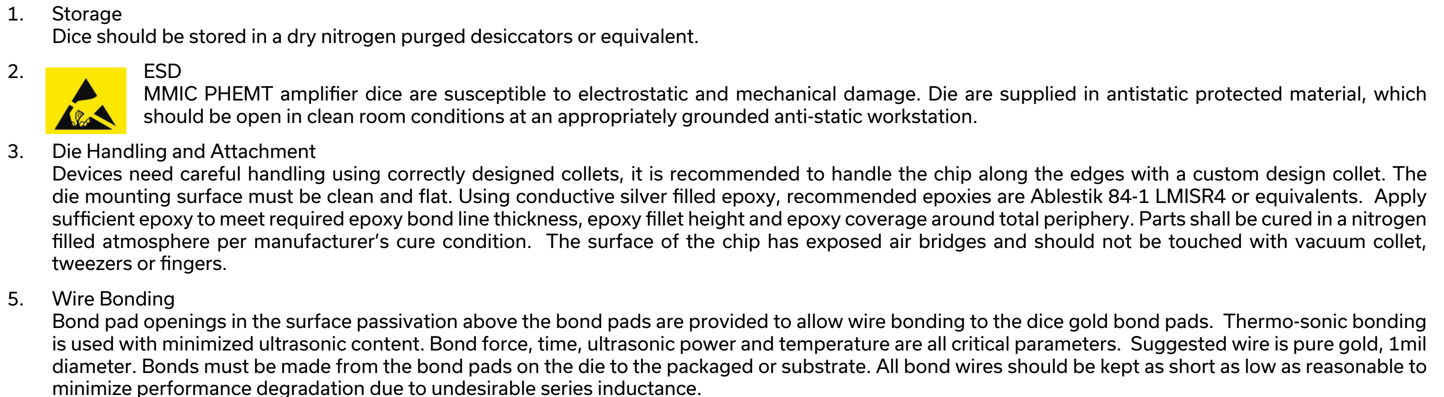
Conditions:
1. VDD=4.5V, IDD = 300mA
2. Gain and Return loss: Pin= -25 dBm
3. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 10 dBm/tone at output.

Switch ON/OFF Sequence:
1. To switch the amplifier ON
   a) Turn ON VG = -2V
   b) Turn ON VDD = 4.5V
   c) Adjust VG Until IDD = 300mA
2. To switch the amplifier OFF
   a) Adjust VG = -2V
   b) Turn OFF VDD
   c) Turn OFF VG

Component	Size	Value	Part Number	Manufacturer
C1-C8	15mil x 15mil	100pF	LSA1515B101M2H5C-F	Presidio
C9, C10	0402	0.1uF	GRM155R71C104KA88D	Murata
C11, C12	1206	10uF	CL31B106KBHNNNE	Samsung

Note: C1-C8 needs to be as close as possible to the die so that we can keep the wire-bonds as short as possible. Short wire-bonds are critical for getting desirable performance.

ASSEMBLY PROCEDURE



1. Storage
   Dice should be stored in a dry nitrogen purged desiccators or equivalent.
2. ESD
   MMIC PHEMT amplifier dice are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic protected material, which should be open in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
   Devices need careful handling using correctly designed collets, it is recommended to handle the chip along the edges with a custom design collet. The die mounting surface must be clean and flat. Using conductive silver filled epoxy, recommended epoxies are Ablestik 84-1 LMISR4 or equivalents. Apply sufficient epoxy to meet required epoxy bond line thickness, epoxy fillet height and epoxy coverage around total periphery. Parts shall be cured in a nitrogen filled atmosphere per manufacturer's cure condition. The surface of the chip has exposed air bridges and should not be touched with vacuum collet, tweezers or fingers.
5. Wire Bonding
   Bond pad openings in the surface passivation above the bond pads are provided to allow wire bonding to the dice gold bond pads. Thermo-sonic bonding is used with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. Suggested wire is pure gold, 1mil diameter. Bonds must be made from the bond pads on the die to the packaged or substrate. All bond wires should be kept as short as low as reasonable to minimize performance degradation due to undesirable series inductance.

ADDITIONAL DETAILED TECHNICAL INFORMATION IS AVAILABLE ON OUR DASH BOARD.

Performance Data	Data Table Swept Graphs S-Parameter (S2P Files) Data Set with and without port extension(.zip file)
Case Style	Die
Die Ordering and packaging information	Quantity, Package — Model No. Small, Gel - Pak: 5,10,50,100 KGD* — AVA-20453MP-DG+ Medium†, Partial wafer: KGD*<1092 — AVA-20453MP-DP+ Full Wafer — AVA-20453MP-DF+ †Available upon request contact sales representative Refer to AN-60-067
Environmental Ratings	ENV80

*Known Good Die ('KGD') means that the dice are taken from PCM Good Wafers and visually inspected according to Mini-Circuits' inspection procedures. While this is not definitive, it does help to provide a higher degree of confidence that the dice are capable of meeting typical RF electrical performance specified by Mini-Circuits.

NOTES

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

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