MMIC DIE

Wideband Amplifier PMA3-15453-D+

50Ω 15 to 45 GHz High Dynamic Range

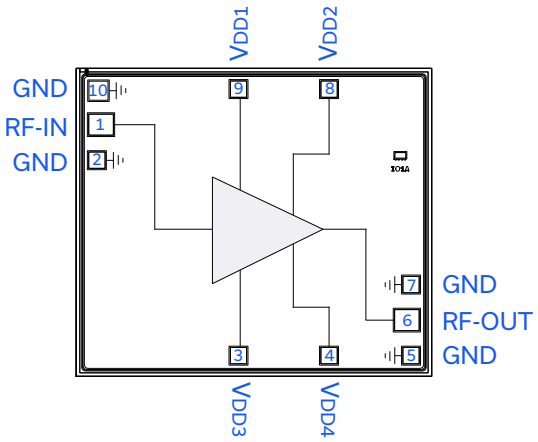
THE BIG DEAL

- Low Noise Figure, Typ. 3.6 dB
- High OIP3, Typ. +24 dBm
- P1dB, Typ. +17 dBm
- +5V Supply Voltage

APPLICATIONS

- Test & Measurement Equipment
- 5G mmWave and Back Haul Radio Systems
- Satellite Communications
- Radar, EW, and ECM Defense systems

FUNCTIONAL DIAGRAM



SEE ORDERING INFORMATION ON THE LAST PAGE

PRODUCT OVERVIEW

The PMA3-15453-D+ is a wideband, low noise MMIC amplifier with a unique combination of high dynamic range and low noise figure over a very broad bandwidth making it ideal for use in a wide variety of transmitter and receiver applications. The device operates from a +5V supply voltage, and is matched to 50 Ohm. The PMA3-15453-D+ die utilizes pHEMT technology and is suitable for chip and wire assemblies.

KEY FEATURES

Features	Advantages
Low Noise Figure, Typ. 3.6 dB	Enables lower system noise figure performance.
High Dynamic Range OIP3, Typ. +24 dBm P1dB, Typ. +17 dBm	Offers low noise figure with correspondingly high P1dB and OIP3 enables flexibility to achieve systems performance with multiple device cascade signal chains
Unpackaged Die	Enables integration into hybrid chip and wire assemblies

REV. OR
ECO-018177
PMA3-15453-D+
MCL NY
230613

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ELECTRICAL SPECIFICATIONS[1] AT +25°C, V_{DD} = +5V, UNLESS NOTED OTHERWISE

Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency Range		15		45	GHz
Gain	15		18.9		dB
	20		17.5		
	30		16.1		
	40		14.4		
	45		11.2		
Output Power at 1 dB Compression (P1dB)	15		+11.8		dBm
	20		+13.4		
	30		+16.9		
	40		+14.2		
	45		+11.1		
Output Third-Order Intercept (P_{OUT} = -5 dBm/Tone)	15		+21		dBm
	20		+23		
	30		+25		
	40		+25		
	45		+25		
Input Return Loss	15		17		dB
	20		11		
	30		13		
	40		11		
	45		15		
Output Return Loss	15		11		dB
	20		11		
	30		11		
	40		13		
	45		15		
Isolation	15-45		40		dB
Noise Figure	15		2.7		dB
	20		2.7		
	30		3.4		
	40		4.2		
	45		5.1		
Device Operating Voltage (V_{DD})		+4.75	+5.0	+5.25	V
Device Operating Current (I_{DD})[2]			128		mA
DC Current Variation vs. Temperature[3]			19.23		µA/°C
DC Current Variation vs. Voltage[4]			0.03		mA/mV

1. Tested in Mini-Circuits Die Characterization Test Board. See Figure 2. Trace and connector losses are de-embedded. Specifications Include the effect of bond wires.
2. Current at P_{IN}= -25 dBm. Increases to 139 mA at P1dB.
3. ((Current at +85°C - Current at -45°C)) / (+130°C)).
4. ((Current at +5.25 V mA)- (Current at +4.75V in mA))/((+5.25V - +4.75V)*1000 mA/mV).

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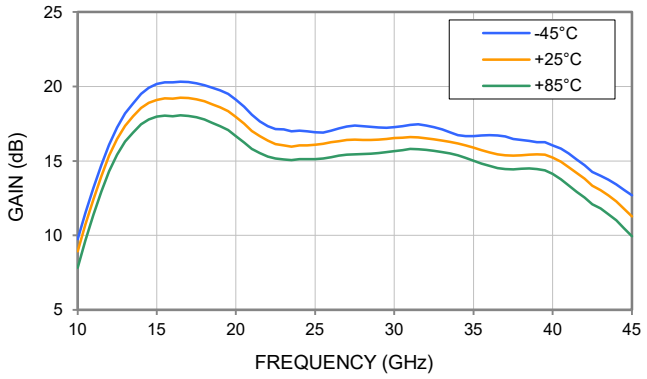
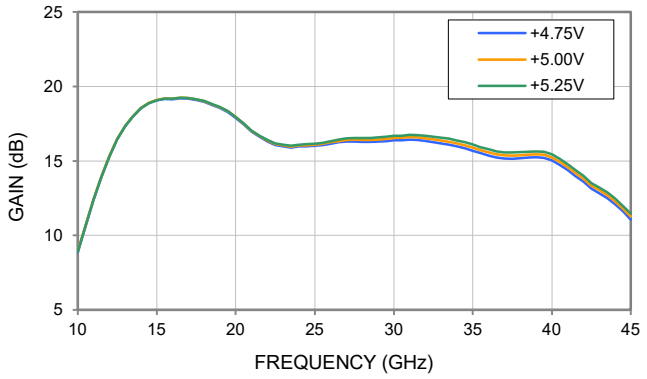
TYPICAL PERFORMANCE GRAPHS

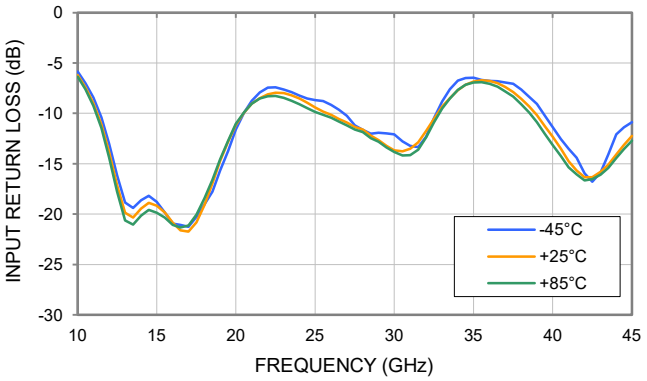
GAIN vs. TEMPERATURE,
P_{IN} = -25 dBm, V_{DD} = +5 V



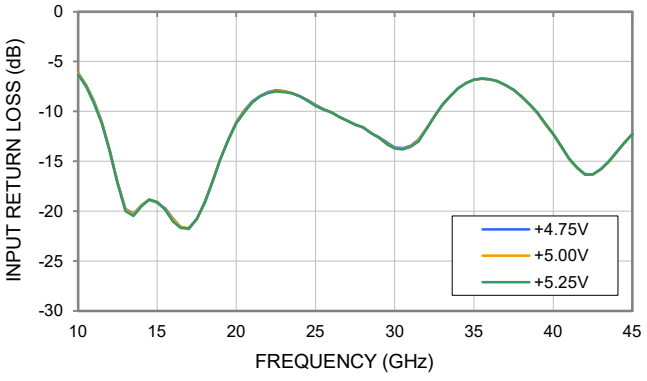
GAIN vs. V_{DD},
P_{IN} = -25 dBm, TEMPERATURE = +25°C



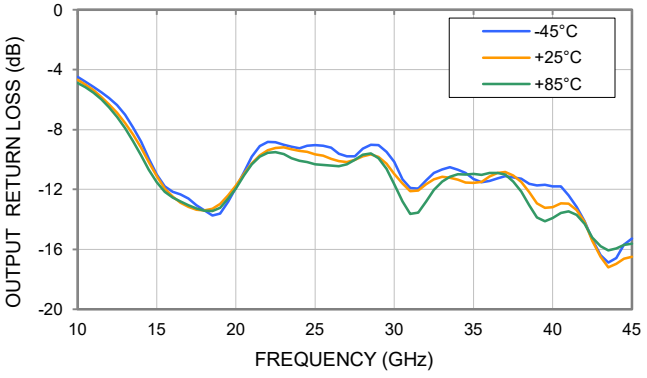
INPUT RETURN LOSS vs.TEMPERATURE,
P_{IN} = -25 dBm, V_{DD} = +5 V



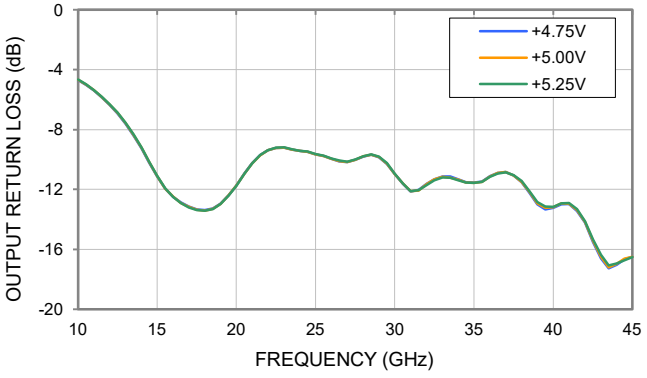
INPUT RETURN LOSS vs. V_{DD},
P_{IN} = -25 dBm, TEMPERATURE = +25°C



OUTPUT RETURN LOSS vs. TEMPERATURE,
P_{IN} = -25 dBm, V_{DD} = +5 V



OUTPUT RETURN LOSS vs. V_{DD},
P_{IN} = -25 dBm, TEMPERATURE = +25°C



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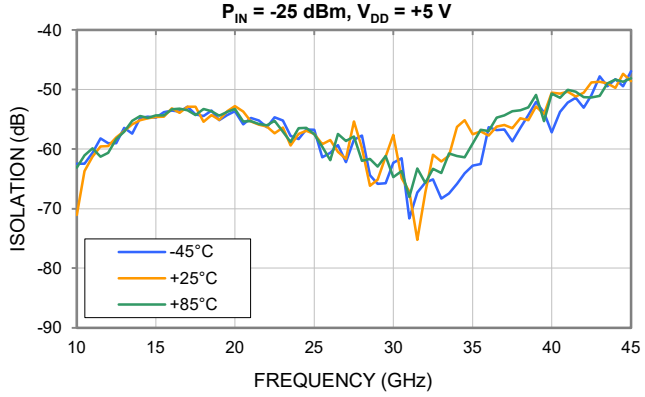
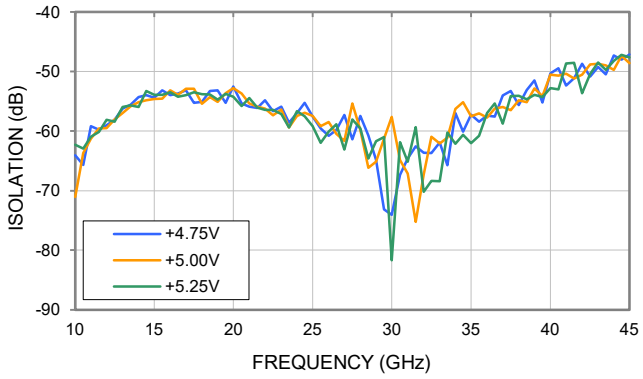
TYPICAL PERFORMANCE GRAPHS

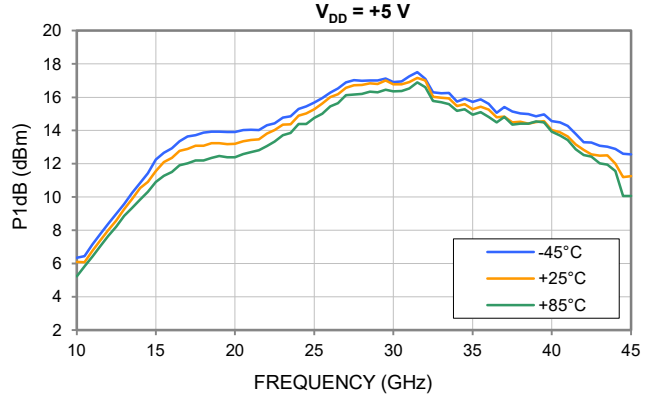
ISOLATION vs.TEMPERATURE,
P_{IN} = -25 dBm, V_{DD} = +5 V



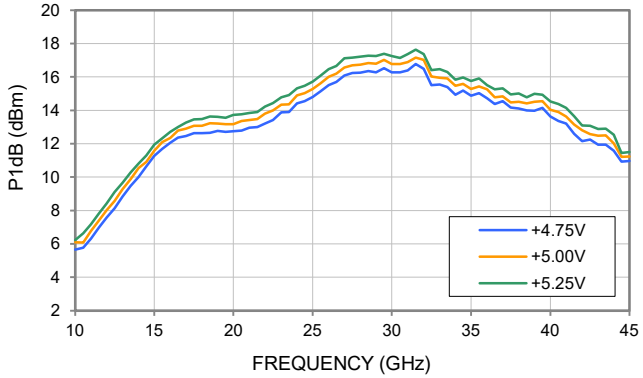
ISOLATION vs. V_{DD},
P_{IN} = -25 dBm, TEMPERATURE = +25°C



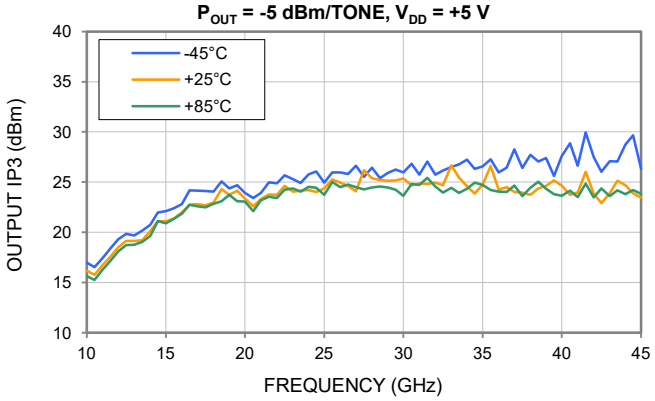
P1dB vs. TEMPERATURE,
V_{DD} = +5 V



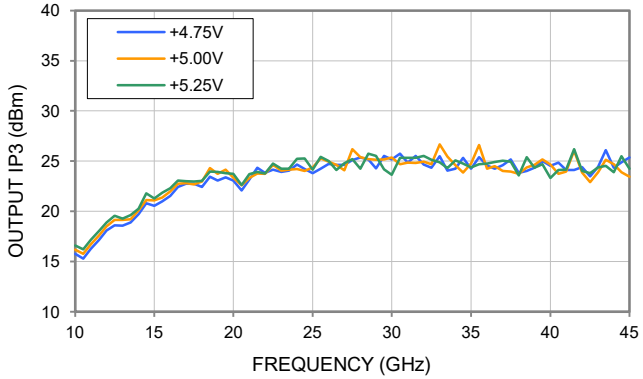
P1dB vs. V_{DD},
TEMPERATURE = +25°C



OUTPUT IP3 vs. TEMPERATURE,
P_{OUT} = -5 dBm/TONE, V_{DD} = +5 V



OUTPUT IP3 vs. V_{DD},
P_{OUT} = -5 dBm/TONE, TEMPERATURE = +25°C



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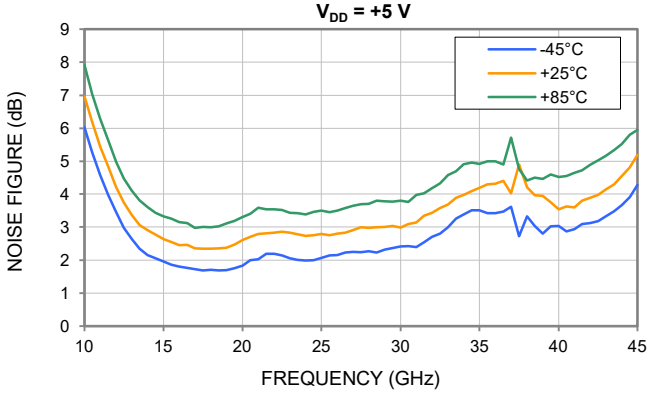
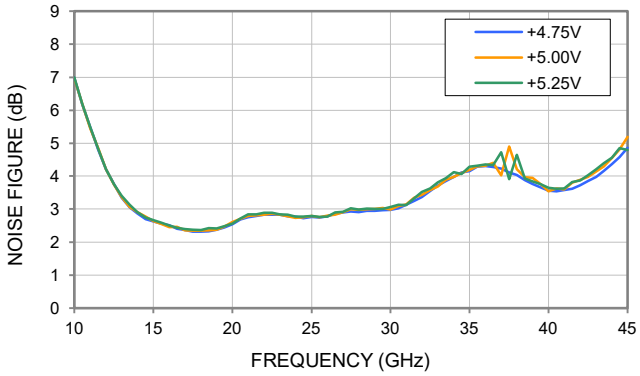
TYPICAL PERFORMANCE GRAPHS

NOISE FIGURE vs. TEMPERATURE, V_{DD} = +5 V



NOISE FIGURE vs. V_{DD}, TEMPERATURE = +25°C



ABSOLUTE MAXIMUM RATINGS[5]

Parameter	Ratings
Operating Temperature	-45 °C to +85 °C
Storage Temperature [6]	+20° C to +35 °C
Junction Temperature[7]	+150 °C
Total Power Dissipation	1.62 W
RF Input Power (CW), V_{DD} = +5V	+23 dBm
DC Voltage at V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}	+10 V

5. Permanent damage may occur if any of these limits are exceeded. Maximum ratings are not intended for continuous normal operation.
6. For die shipped in Gel-Pak see ENV-80 (limited by packaging).
7. Peak temperature on Top of Die.
6. For die shipped in Gel-Pak see ENV-80 (limited by packaging)

THERMAL RESISTANCE

Parameter	Ratings
Thermal Resistance (Θ_{jc})[8]	32.2 °C/W

8. Θ_{jc}= (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

ESD RATING[9]

	Class	Voltage Range	Reference Standard
Human Body Model (HBM)	1A	250V to < 500V	ANSI/ESDA/JEDEC JS-001-2017

ESD HANDLING PRECAUTION: This device is designed to be Class 1A for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage.

9. Tested in 3x3mm 12-lead QFN-Style Package

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FUNCTIONAL DIAGRAM

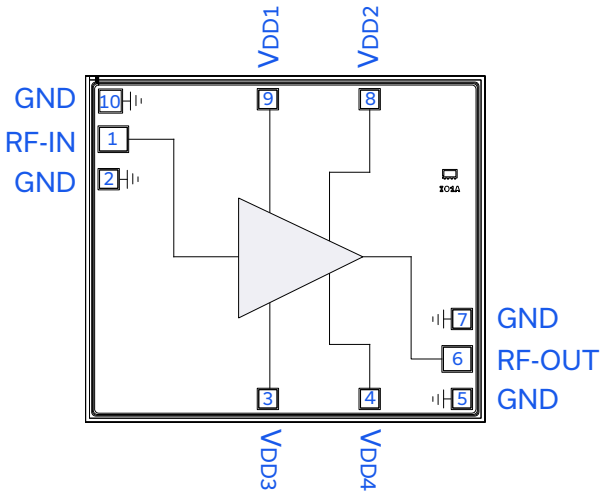

Figure 1. PMA3-15453-D+ Functional Diagram

PAD DESCRIPTION

Function	Pad #	Application Description (Refer to Figure 1)
RF-IN	1	RF Input Port
RF-OUT	6	RF Output Port
V_{DD1}	9	Voltage Input Port 1
V_{DD2}	8	Voltage Input Port 2
V_{DD3}	3	Voltage Input Port 3
V_{DD4}	4	Voltage Input Port 4
GND	2, 5, 7, 10	Connected to die backside through vias. Bond wires to ground are optional

DIE OUTLINE: inches [mm], Typical

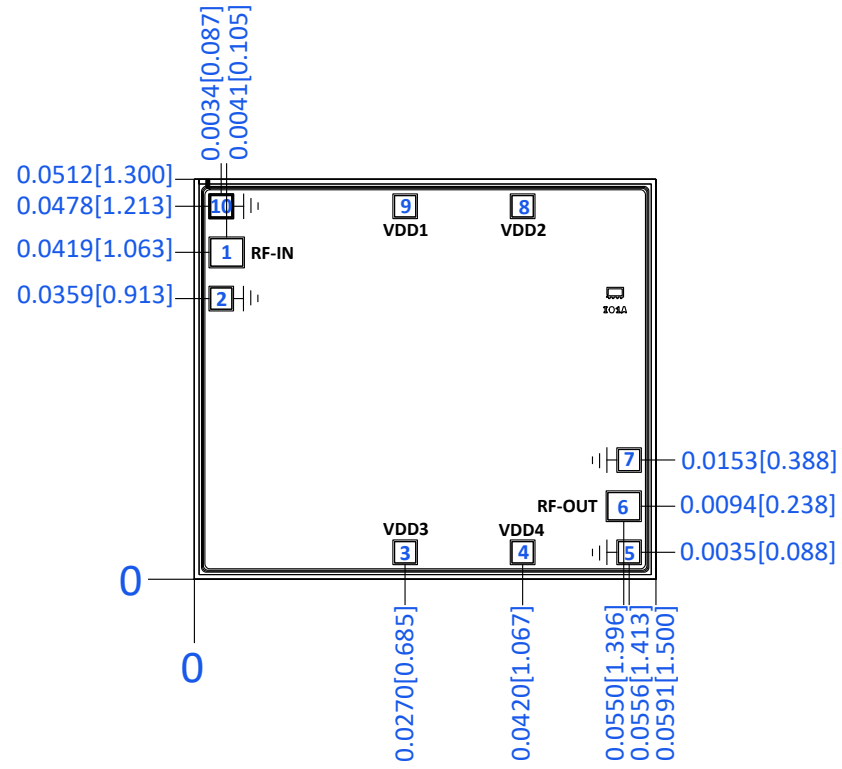

Figure 2. PMA3-15453-D+ Die Outline

DIMENSIONS: inches [mm], Typical

Die Size	0.0591 x 0.0512 [1.500 x 1.300]
Die Thickness	0.0039 [0.100]
Bond Pad Sizes:	
Pads 2–5, 7–10	0.0027 x 0.0027 [0.069 x 0.069]
Pad 1 & 6	0.0041 x 0.0035 [0.104 x 0.089]
Plating (Pads & Bottom of Die)	Gold

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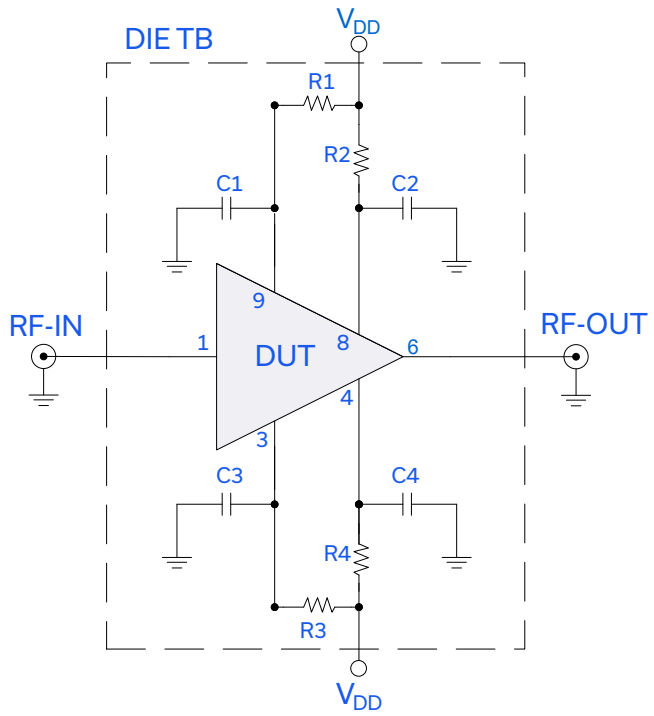
CHARACTERIZATION AND APPLICATION CIRCUIT



Electrical Parameters and Conditions
1. Gain and Return Loss: P_{IN}= -25 dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, -5 dBm/ tone at output.
3. V_{DD} = +5V

Figure 3. PMA3-15453-D+ Characterization and Application Circuit

Component	Value	Size	Part Number	Manufacturer
R1, R3	39 Ω	0603	SG73P1JTTD39R0F	KOA
R2 , R4	24 Ω	0603	SG73S1JTTD24R0F	KOA
C1, C2, C3,C4	100 pF	0402	GRM1555C1H101JA01D	Murata

ASSEMBLY DIAGRAM

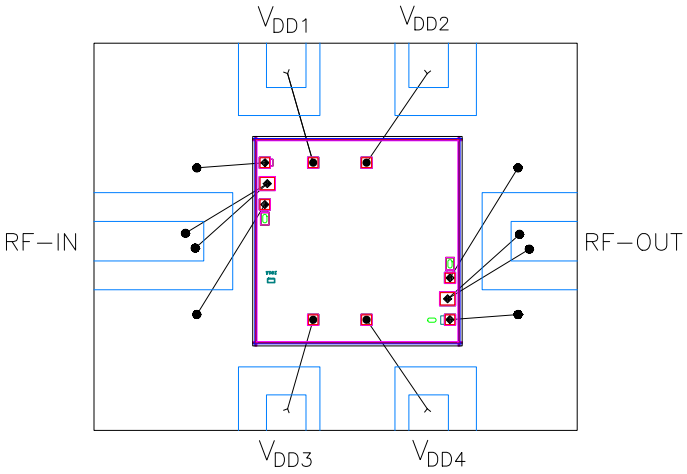


Figure 4. PMA3-15453-D+ Assembly Diagram

Refer to the table in Figure 3. for more details on the passive components

- Bond wire diameter: 1 mil
- Bond wire lengths from Die Pad to PCB at RF-IN & RF-OUT ports: 26 ± 2 mils
- Typical Gap from Die edge to PCB edge: 3 mils
- PCB thickness and material: 6.6 mil Rogers RO4350B (Thickness: 1 oz copper on each side).

ASSEMBLY AND HANDLING PROCEDURE

1. Storage
   Die should be stored in a dry nitrogen purged desiccator or equivalent.
2. ESD Precautions
   MMIC pHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in anti-static protected material, which should be opened only in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
   Devices require careful handling using tools appropriate for manipulating semiconductor chips. It is recommended to handle the chips along the edges with a custom designed collet. The surface of the chips have exposed air bridges and should not be touched with a vacuum collet, tweezers or fingers.
   The die mounting surface must be clean and flat. Using conductive silver-filled epoxy, apply sufficient adhesive to meet the required bond line thickness, fillet height and coverage around the total periphery of the device. The recommended epoxy is Ablestik 84-1 LMISR4 or equivalent. Parts should be cured in a nitrogen-filled atmosphere per manufacturer's recommended cure profile.
4. Wire Bonding
   Openings in the surface passivation above the gold bond pads are provided to allow wire bonding to the die. Thermosonic bonding is recommended with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. The suggested interconnect is pure gold, 1 mil diameter wire . Bonds are recommended to be made from the bond pads on the die to the package or substrate. All bond wire length and bond wire height should be kept as short as possible, unless specified by design, to minimize performance degradation due to undesirable series inductance.

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ADDITIONAL DETAILED INFORMATION IS AVAILABLE ON OUR DASH BOARD CLICK HERE

Performance Data	Table Graphs S-Parameter (S2P Files) Data Set (.zip file)	
Case Style	Die	
RoHs Status	Compliant	
Die Ordering and Packaging Information	Quantity, Package	Model No.
	Gel - Pak: 5, 10, 50, 100 KGD*	PMA3-15453-DG+
	Medium†, Partial wafer: KGD*<928	PMA3-15453-DP+
	Full wafer†	PMA3-15453-DF+
	†Available upon request contact sales representative. Refer to AN-60-067	
Die Marking	IO1A	
Environmental Ratings	ENV80	

* Known Good Die ("KGD") means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within a predefined range. While DC testing is not definitive, it does provide a higher degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.