MMIC DIE

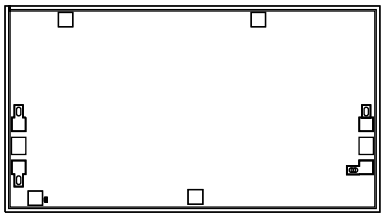
Wideband Amplifier

AVA-2183-D+

50Ω 2 to 18 GHz

THE BIG DEAL

- Wideband, 2 to 18 GHz
- Flat Gain 16.6±0.7 dB from 2 to 18 GHz
- P1dB, +19.6 dBm Typ. at 10 GHz.
- OIP3, +27.4 dBm Typ. at 10 GHz.



+RoHS Compliant
The +Suffix identifies RoHS Compliance.
See our website for methodologies and qualifications

SEE ORDERING INFORMATION ON THE LAST PAGE

APPLICATIONS

- 5G MIMO and Back Haul Radio Systems
- Satellite Communications
- Test and Measurement Equipment
- Radar, EW, and ECM Defense Systems

PRODUCT OVERVIEW

The AVA-2183-D+ is an amplifier die that operates from 2 to 18 GHz that is fabricated on a GaAs PHEMT MMIC process. The Amplifier provides 16.6 dB of Gain, +27.6 dBm OIP3 and +19.7 dBm Output Power at 1 dB Compression point with 16 dB typical Return Loss while requiring +4V and 210 mA DC power. Gain flatness is +/- 0.7 dB across the operating bandwidth. The Amplifier is ideal for use in very wideband ECM, Test & Measurement and Microwave communications systems.

KEY FEATURES

Feature	Advantages
Wideband: 2 to 18 GHz • 16 dB Gain Typ. at 2 GHz • 17 dB Gain Typ. at 18 GHz	Suitable for wide bandwidth defense and test and measurement application as well as narrow band performance driven applications.
Good P1dB & OIP3 • +19.6 dBm P1dB Typ. at 10 GHz • +27.4 dBm OIP3 Typ. at 10 GHz	Suitable as a driver amplifier in receiver/transmitter chains.
High Reverse Isolation	Isolates adjacent circuitry without need for an external expensive isolator.
Input and Output Return Loss	Eliminates need for external matching circuit providing published Return Loss.
Unpackaged Die	Suitable for chip and wire hybrid assemblies.

REV. OR
ECO-014455
AVA-2183-D+
MCL NY
230710

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ELECTRICAL SPECIFICATIONS[1] AT 25°C, VDD=+4V, IDD=210mA & Zo=50Ω UNLESS NOTED OTHERWISE

Parameter	Condition (GHz)	VDD=+4V Min.	VDD=+4V Typ.	VDD=+4V Max.	Units
Frequency Range		2		18	GHz
Gain	2		15.9		dB
	5		16.1		
	10		17.2		
	15		16.7		
	18		16.9		
Input Return Loss	2		12		dB
	5		16		
	10		14		
	15		11		
	18		14		
Output Return Loss	2		18		dB
	5		20		
	10		19		
	15		16		
	18		15		
Reverse Isolation	2 - 18		47.4		dB
Output Power at 1dB Compression	2		18.9		dBm
	5		19.3		
	10		19.6		
	15		18.2		
	18		17.6		
Output Third-Order Intercept (Pout = 0 dBm/Tone)	2		31.2		dBm
	5		29.1		
	10		27.4		
	15		25.2		
	18		23.7		
Noise Figure	2		6.8		dB
	5		6.4		
	10		5.5		
	15		4.7		
	18		5.1		
Device Operating Voltage (VDD)			+4		V
Device Operating Current (IDD)			210		mA
Device Gate Voltage (VGG)			-0.46		V
Device Gate Current (IGG)			-0.2		µA
Thermal Resistance, Junction-to-Ground Lead (ΘJC)			38.8		°C/W

1.Die is soldered and measured on Mini-Circuits die characterization board. See characterization circuit (Fig. 1).

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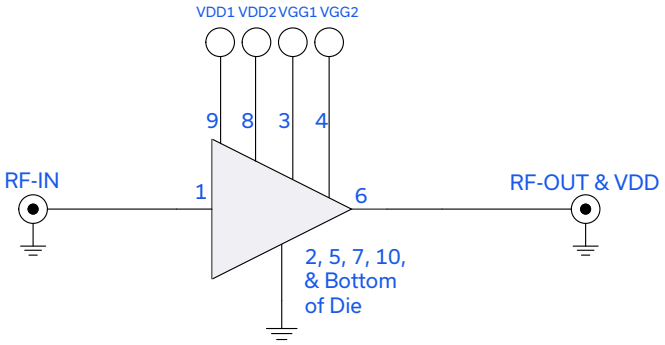
MAXIMUM RATINGS[2]

Parameter	Ratings
Operating Temperature (ground lead)	-40°C to +85°C
Junction Temperature	+150°C[3]
Power Dissipation	1.7W
Input Power (CW)	+23 dBm (5 minute max) +14 dBm (continuous)
DC voltage on RF-OUT	+7V
Current IGG	-5mA to 0mA
Current IDD	320mA
DC Voltage on V_{DD} (V_{DD1} & V_{DD2})	+7V
DC Voltage on V_{GG} (V_{GG1} & V_{GG2})	-1.5 V to -0.2 V

2. Permanent damage may occur in any of these limits are exceeded. Electrical maximum ratings are not intended for continuous normal operation.

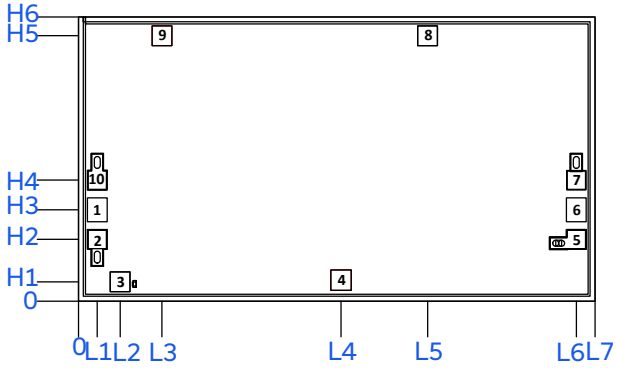
3. Tj = +85°C + (VDD)*(IDD)*(ΘJC) = +117°C. Keeping Tj below +117°C will ensure MTTF > 100 Years.

SIMPLIFIED SCHEMATIC AND PAD DESCRIPTION



Function	Pad Number	Description
RF-IN	1	RF Input Pad
GROUND	2, 5, 7, 10, & Bottom of die	The bond pads are connected to backside through vias and do not require wire-bond connections to ground.
VGG1	3	Gate Bias Pad #1
VGG2	4	Gate Bias Pad #2
RF-OUT	6	RF Output Pad
VDD2	8	Drain Bias Pad #2
VDD1	9	Drain Bias Pad #1

BONDING PAD POSITION



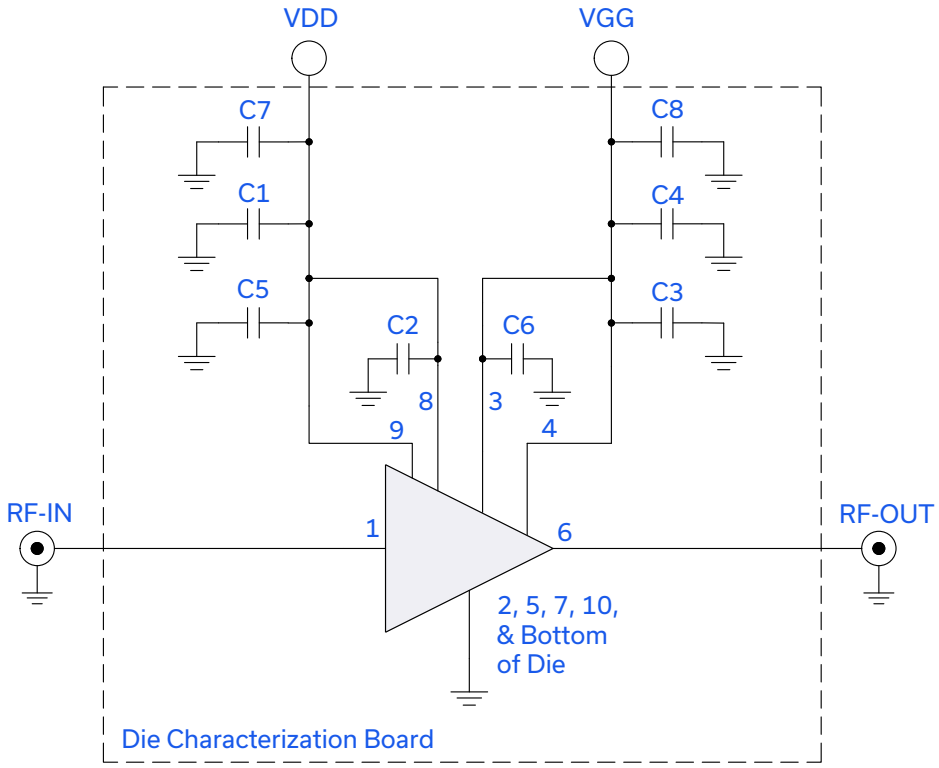
DIMENSION IN µM, TYP.

L1	L2	L3	L4	L5	L6	L7
95	211	422	1328	1767	2519	2614

H1	H2	H3	H4	H5	H6
98	312	462	612	1343	1438

Thickness	Die size	Pad size 1 & 6	Pad size 2,3,5,7,8,9 & 10	Pad size 4
100	2614 x 1438	93 x 113	93 x 93	96 x 96

CHARACTERIZATION & APPLICATION CIRCUIT



Component	Size	Value	Part Number	Manufacturer
C2, C3, C5 & C6	100pF	22x22mil	MA4M3100	MACOM
C1 & C4	0.1uF	0402	GRM155R71A474KE01D	Murata
C7 & C8	10uF	1206	CL31B106KBHNNNE	Samsung

Fig.1: Characterization & Application Circuit
Note: This block diagram is used for characterization (Die is attached and wire-bonded on a die characterization test board). Gain, Return Loss, Output Power at 1dB Compression (P1dB), Output IP3 (OIP3) and Noise Figure are measured using Agilent's N5242A PNA-X Microwave Network Analyzer.

Conditions:
1. VDD = +4V
2. VG is set to obtain desired IDD as shown in specification table.
3. Gain and Return Loss: Pin = -25 dBm
4. Output IP3 (OIP3): Two Tones, spaced 1 MHz apart, 0 dBm/Tone at Output.

Power ON Sequence:
1) Set VGG = -1.3V. Apply VGG.
2) Set VDD = +4V. Apply VDD.
3) Increase VGG to obtain desired IDD as shown in specification table.
4) Apply RF Signal

Power OFF Sequence:
1) Turn off RF Signal.
2) Adjust VGG down to -1.3V.
3) Turn off VDD.
4) Turn off VGG.

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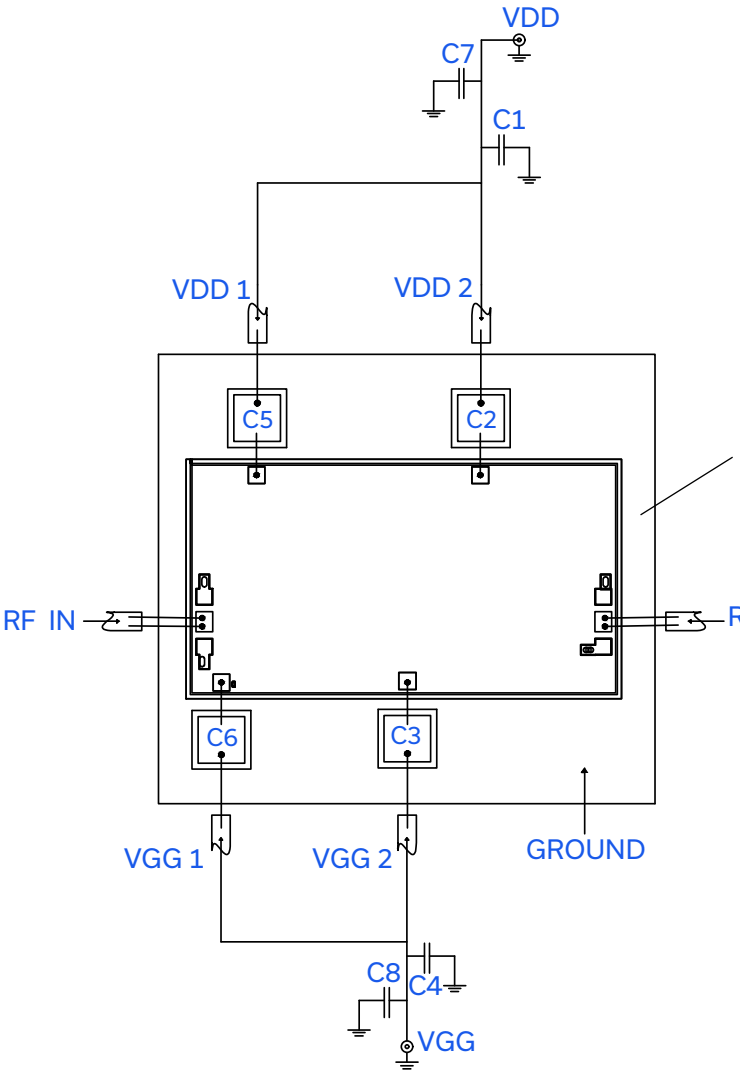
ASSEMBLY DIAGRAM



Note: Tested on die characterization board with following bond lengths:
1. Typical bond length for RF-IN: 280µm (11mils)
2. Typical bond length for RF-OUT: 280µm (11mils)
3. Typical bond lengths from die, capacitor, VDD1, VDD2, VGG1, and VGG2 were kept as short as possible
4. Component list given in Figure 1.

Typical gap of 76µm (3mils) between the edge of the die and edge of the ground pad.

ASSEMBLY AND HANDLING PROCEDURE

1. Storage
   Die should be stored in a dry nitrogen purged desiccators or equivalent.
2. ESD
   MMIC PHEMT amplifer die are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic protected material, which should be open in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
   Devices need careful handling using correctly designed collets, it is recommended to handle the chip along the edges with a custom design collet. The die mounting surface must be clean and flat. Using conductive silver filled epoxy, recommended epoxies are Ablestik 84-1 LMISR4 or equivalents. Apply sufficient epoxy to meet required epoxy bond line thickness, epoxy fillet height and epoxy coverage around total periphery. Parts shall be cured in a nitrogen filled atmosphere per manufacturer's cure condition. The surface of the chip has exposed air bridges and should not be touched with vacuum collet, tweezers or fingers.
4. Wire Bonding
   Bond pad openings in the surface passivation above the bond pads are provided to allow wire bonding to the Die gold bond pads. Thermo-sonic bonding is used with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. Suggested wire is pure gold, 1mil diameter. Bonds must be made from the bond pads on the die to the packaged or substrate. All bond wire length and bond wire height should be kept as short as possible unless specified by the Assembly Drawing to minimize performance degradation due to undesirable series inductance.

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ADDITIONAL DETAILED TECHNICAL INFORMATION IS AVAILABLE ON OUR DASH BOARD.

Performance Data	Data Table Swept Graphs S-Parameter (S2P Files) Data Set with and without port extension(.zip file)
Case Style	Die
Die Ordering and packaging information	Quantity, Package — Model No. Gel - Pak: 5,10,50,100 KGD* — AVA-2183-DG+ Medium†, Partial wafer: KGD*<570 — AVA-2183-DP+ Full wafer — AVA-2183-DF+ †Available upon request contact sales representative Refer to AN-60-067
Die Marking	EL-AMP-11-2
Environmental Ratings	ENV80

*Known Good Die ("KGD") means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within a predefined range. While DC testing is not definitive, it does provide a higher degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

NOTES

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

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