



# Frequently Asked Questions – DAT & ZX76 Series Digital Step Attenuators

#### 1. What is the definition of "Switching Control Frequency"?

The switching control frequency is the frequency of the control signals. For the DAT and ZX76 models, the switching control frequency is the frequency of Latch Enable (LE). The frequency is defined in the datasheets with the limitation being the time required to allow all the internal registers of the DAT to be set to the required values and the attenuator to settle to its new value.

#### 2. What is the maximum Switching Control Frequency?

Maximum switching control frequency is dependent upon the model type:

For single supply (positive voltage) versions (-PP,-SP):25 kHzFor dual Supply (positive and negative voltage) versions: (-PN, -SN):1 MHz

If this switching frequency is exceeded the switching speed (defined as 50% control to 0.5dB of final value) will be affected. For example, in the single supply serial controlled versions; the switching speed is ~500nS at a switching frequency of 25 KHz, and increases to ~1.5 $\mu$ S at a switching frequency of 300 KHz. The above characteristic is caused by the internal Negative Voltage Generator operation. Please note that models with dual supply voltages do not have this issue and switching speed is not degraded when the switching frequency is increased above 25 KHz up to 1 MHz.

#### 3. How do I calculate bit switching time and total switching time for these attenuators?

Bit switching time and total switching time are different for serial controlled and parallel controlled models.

For **serial controlled** models bit switching and total switching time are dependent on the external (customer supplied) clock but the minimums are:

 $\label{eq:period} \begin{array}{l} \hline Per \ Bit \ switching \ time: \\ \hline Serial \ data \ set-up \ time \ before \ clock \ rising \ edge \ t_{SDSUP} = 10nS \\ \hline Serial \ clock \ HIGH \ time \ t_{clkH} = 30nS \\ \hline Serial \ data \ hold \ time \ after \ clock \ falling \ edge \ t_{SDHLD} = 10nS \\ \hline Serial \ clock \ LOW \ time \ t_{clkL} = 30nS \\ \end{array}$ 



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So, total minimum time for each bit = 80nS

Total switching time (6 bit model):

Total minimum time for 6 bits =  $80nS \times 6 = 480nS$ Minimum LE set-up time after last clock falling edge  $t_{LESUP} = 10nS$ LE transient switching time=~400nS So, total minimum time to change attenuation state for serial controlled model=~900nS

For **parallel controlled** models there is no external clock and the minimum switching times are computed as follows:

Bit switching time:

Parallel data set-up time before rising edge of LE  $t_{PDSUP} = 10nS$ LE minimum pulse width  $t_{LEPW} = 10nS$ Parallel data hold time after clock falling edge  $t_{PDHLD} = 10nS$ So, total minimum time bit switching time = 30nS

Total switching time:

Total minimum bit switching time = 30nS LE transient switching time=~400nS So, total minimum time to change attenuation state for parallel controlled model=~430nS

See timing diagrams in individual data sheets for more information on bit switching time.

#### 4. What is the function of the Latch Enable (LE) bit in serial or parallel control models?

#### Serial control models

The attenuator is controlled by three control lines: DATA, CLOCK, and Latch Enable (LE). The DATA and CLOCK enter a binary code into a shift register in the attenuator that defines the attenuation value of the attenuator. Once the code has been entered when LE is HIGH it executes the binary code. When LE is LOW, attenuation is latched and can not be changed. The LE should be LOW while binary code is entered to prevent the attenuator value from changing. The LE input should then be toggled HIGH and brought LOW again, latching the new data.

#### Parallel control models

There are two available programming modes for DAT:

Latched parallel programming Direct parallel programming

**For latched parallel programming,** the Latch Enable should be held LOW while changing attenuation state control values, then toggled to HIGH level to set the attenuation value and brought LOW again to latch the new attenuation state.

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For direct parallel programming, the Latch Enable line is set HIGH. Changing attenuation state control values will change device state to new attenuation value immediately. Direct mode is ideal for manual control of the device.

#### 5. How should the "Power Up Control" Pins of the serial DAT models be connected?

The "Power Up Control" Pins define the initial attenuation state when DC Voltage ( $V_{DD}$ ) is applied to the device. When the "Power-up Control" pins are connected to ground directly or through  $10K\Omega$  resistors, the initial attenuation value is set to 0dB. To get a different initial attenuation value you have to connect V<sub>DD</sub> to the appropriate "Power-up Control" pins C0.5 – C16 as shown in the datasheets.

We recommend using  $10k\Omega$  resistors between power up control pins and ground. These resistors will minimize the parasitic resonances at high frequencies caused by the small attenuator package and improve the attenuation accuracy at high frequencies.

#### 6. What is the function of PUP1 and PUP2 in the parallel controlled DATs?

The PUP pins are the CMOS gates with no current sink or source. They must be connected directly to V<sub>DD</sub> or GND for proper Power-Up operation. If not, the voltage on the gates will float to a random value giving random initial attenuation values. To drive the PUP pins with control signals the customer can use a Pull-up or Pull-down scheme using resistor values from  $0\Omega$  to 100kΩ.

#### 7. Is it possible to determine start up attenuation of a ZX76 series model such as ZX76-31-SP+?

In serial controlled ZX76 attenuators such as ZX76-31-SP+ it is not possible to set start-up attenuation other than 0dB. However in parallel controlled ZX76 models such as ZX76-31-PP+ it can be done by using software or external hardware; for example, using pullup series resistors on each control line. The ZX76 models do not have an internal Power-Up provision due to space limitation of the package

#### 8. What is the attenuation state of the attenuator during transition between specified attenuation states?

During transition between specified attenuation states the attenuation of a DAT of ZX76 series attenuator is undetermined and can even reach minimum attenuation (Insertion loss) momentarily.

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#### 9. What are pin 7&8 connections for serial DAT models?

For serial controlled DAT models such as the DAT-31R5-SP+ the state of pins 7 & 8 is not important. They can be connected to either '0' (GND), '1' (VCC) or left unconnected with no effect on the model's performance.

## 10. What is the function of the $10k\Omega$ series resistors on pins 1 & 3 of the DATs and why do we need to connect the resistors also for models where these pins are listed as N/C such as DAT-15R5-PP+ ?

The  $10k\Omega$  series resistors improve attenuation accuracy resulting from package parasitic. Even in models where pins 1 & 3 are not used, package parasitic may degrade attenuation accuracy at high frequency due to the close proximity of these pins to the RFin pin and therefore we recommend connecting these pins to ground via  $10k\Omega$  resistors.

### 11. Why do the DAT models have two $V_{DD}$ pins? Can the model be powered from either pin 6 or pin 9? Must both these pins be tied to $V_{DD}$ ?

Both pins must be connected to  $V_{DD}$  for proper operation.

# 12. In the DAT models, can the GND pins be left open if the "paddle ground" is properly grounded? If these pins must be grounded, then can I simply connect them to the "paddle ground"?

In general, it is always a good practice to separate RF ground and digital ground in MMIC designs. Specific to the DAT series, to achieve the performance specified in our datasheets, the device must be configured with all GND pins soldered to ground as shown in the PCB Layout drawing.

#### 13. How should pin 20 be connected in DAT models with a 1dB step such as DAT-31-PN+?

Pin 20 is reserved for models with 0.5dB step which use the same case style as models with 1 dB step such as DAT-31-PN+. For models with 1dB step, we recommend connecting this pin to ground through a  $10k\Omega$  resistor. Do not apply control voltage to this pin as it may result in unknown attenuation state.

# 14. What is the function of the parallel resistor and capacitor on the LE and Control lines on parallel control model test boards and the LE, CLOCK and DATA lines on serial control model test boards?

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The resistor and capacitor form a RC filter which filters external noise entering the DAT from the control line.

#### 15. Can I use 5V power supply to power the DAT or ZX76 series models?

Yes, however you need to use a resistive voltage divider or LDO (low drop-out voltage regulator) to reduce the voltage as  $V_{DD}$  over 4V may cause permanent damage. See Application Note AN-70-004 for detailed information on this.

#### 16. Can DAT-31R5-SP/ PP be used at 5V through a 30k $\Omega$ resistor?

DAT models can draw up to 2mA surge current. The  $30k\Omega$  value is too high and will result in a significant voltage drop during startup and transition that can cause the DAT to lock-up.

For detailed information about this subject see Application note 70-004 <u>http://www.minicircuits.com/pages/pdfs/an70004.pdf</u> and answer to question 15 above.

#### 17. Can the attenuators be damaged if negative voltage of $V_{DD}$ is less then -0.3?

Yes. Exceeding any of the maximum ratings noted in the data sheet can damage the unit.

#### 18. Can I use the DAT models with a negative power supply?

Yes, but you need to use a DUAL power supply model with both negative & positive voltage:  $V_{SS}$ = -3V,  $V_{DD}$ = +3V Please use the models with the suffix "-SN" or "-PN"

### 19. Regarding PCB design, if the $10k\Omega$ series resistors on control lines C0.5 – C16 are omitted can pins 1, 20, 19, 17, 16, 15 be connected directly to GND?

If the resistors are omitted and pins 1,20, 19, 17, 16, 15 are connected directly to GND, the DAT attenuation state is not changed, however some accuracy degradation is possible because these resistors minimize the parasitic resonances at high frequencies caused by the small size of the attenuator package.

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#### 20. Is it possible to connect DAT or ZX76 series attenuators in cascade without a DC block capacitor between stages?

Yes. Neither the DAT nor ZX76 series models produce DC voltage at the RF ports and can be cascaded without coupling capacitors at the RF ports as long as there is no DC voltage on the RF line.

#### 21. Are the input and output interchangeable?

Yes. It is possible to use either RF port as input or output in both the ZX76 and DAT series attenuators, however the specifications are guaranteed for the RFin and RFout as noted in the data sheet. There might be minor changes in the performance when input and output ports are reversed.

#### 22. What is the noise level generated by the single positive supply voltage DAT and ZX76 attenuators?

The single supply models (-SP, -PP suffix) have an internal generator producing negative voltage. This allows powering these devices from single positive voltage source. The noise level of the generator is typically lower than -120dBm, noise level of dual supply models (-PN, -SN suffix) is much lower.

#### 23. Are there any advantages to using dual supply voltage DAT or ZX76 models?

Yes. Dual supply voltage models can operate with a switching frequency up to 1MHz with no degradation of switching speed, as opposed to single supply voltage models which begin to show switching speed degradation at switching frequencies over 25kHz.

Additionally, the dual supply voltage models feature lower noise level and less spurious signals at the RF output than single voltage supply models. This is caused by the internal negative voltage generator used in the single voltage supply models.

#### 24. What is the noise figure of the DAT and ZX76 attenuators?

The NF is approximately equal to the total loss of the attenuator (insertion loss of the device + current attenuation setting).

#### 25. If V<sub>DD</sub> is lower than the Control Voltage can it cause problems?

Having V<sub>DD</sub> lower than the control voltage will not cause problems in ZX76 models since they contain internal buffer circuitry which limits the control signals to below V<sub>DD</sub>.





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In the DAT models  $V_{DD}$  lower than the control voltage will cause problems, therefore we recommend adding external resistor voltage dividers or Schmitt triggers between the CPU and DAT to reduce the control voltages to  $V_{DD}$  or less.

Please see the schematic below with suggested resistor's values for the resistor dividers. The current consumption of the dividers shown is very low (~13uA) and should not be a problem for a typical CPU.



Figure 1

### 26. Is it possible to use more than one DAT or ZX76 attenuator in cascade and if so how can they be controlled?

Yes, it is possible to use two or more attenuators in cascade - please see schematics below. At high attenuation values interaction due to VSWR and leakage through external circuit may limit attenuation accuracy.

Regarding control, using multiple LE line you can latch several attenuators in cascade and change the attenuation of one at a time, by applying "1" logic to the appropriate LE pin. Please note that for ZX76 models all digital pins are in the same J1 port and they need to be separated to the appropriate data bus after the interface connector. See figures 2 & 3 below.















#### 27. What role do the inverting Schmitt triggers play in the evaluation board circuits?

They filter external noise and limit the control voltage to a level lower than  $V_{DD}$ . In our test boards we use paired serial inverting Schmitt triggers to get a non-inverted signal. You don't have to use Schmitt triggers in your application if you have low noise control lines and the control high level is lower than  $V_{DD}$ . If you need the buffer you can use a smaller non-inverting trigger.

#### 28. How can the noise signals such as power noise and clock noise be reduced?

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To reduce external noise on control lines we recommend using Schmitt trigger buffers and RC filters. The time response of the filter depends on the required switching time: large capacitors decrease noise significantly but increase the switching time while smaller capacitors will have less effect on the switching time but do not decrease the noise as much.

You may also consider using dual power supply (-PN & -SN suffix) models which have a lower noise level.

#### 29. How can I control multiple attenuators?

There are two options to control multiple attenuators, with the number controllable simultaneously limited by the number of control lines available. For example, if you are using a PC's LPT port, 12 control lines are available (although some of them use negative logic and will need to be programmed accordingly) while a dedicated I/O card will have many more.

- Option1: Allows changing of only one attenuator at a time. In this case, you connect the same data lines (or single data line and one CLOCK for serial controlled attenuators) to all the units and independent LE (Latch Enable) control signals for each attenuator (see figures 5 &6 above for reference). Thus, using the LPT port you can control up to 10 serial interface units (10 LE lines + 1 line for DATA + 1 line for CLOCK = 12 control lines) or seven 5-bit parallel controlled units (7 LE lines +5 parallel data lines=12 control lines).
- Option 2: Each attenuator can be controlled independently or simultaneously with other attenuators. To implement this option you need separate lines for each LE and DATA lines. Thus with the PC's LPT you can control only five serially controlled models (5 LE lines + 5 DATA lines + 1 CLOCK for all units = 11 control lines) or a pair of 5-bit parallel controlled units (5 parallel DATA lines X 2 units + 2 LE lines=12 control lines).

We highly recommend using Schmitt Triggers on the control lines going to DAT models in order to limit input control voltage of the DAT to below  $V_{DD}$  when using I/O cards capable of producing higher voltages. For the ZX76 models, which include internal Schmitt triggers such a precaution is not needed.

#### 30. What should the LPT pin configuration be to control a DAT or ZX76 model?

In general the LPT can be used in a wide variety of configurations to control one or more attenuators, and require different configurations for parallel or serial controlled models. Any of pins 1-9 or 17 can be used for CLOCK, LE, DATA or C0.5-C16 and pins 18-25 for GND. Pins 16 and 14 can also be used for CLOCK, LE, DATA or C0.5-C16 however they operate using negative logic ('1'=0V, '0'=5V) and must be programmed accordingly.

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The free evaluation software available for download from Mini-Circuits' web site at: http://yoni.minicircuits.com/downloads/DigitalStepAtt CD.zip (DAT models) http://yoni.minicircuits.com/downloads/DigitalStepAtt\_ZX76\_CD.zip (ZX76 models) Please note that the software assumes the same pin configuration used by accessory cable ZX76-CS+ (for serial control) and ZX76-CP+ (for parallel control). Pinout is shown ZX76 catalog data sheets.

#### 31. Can a Digital Step Attenuator be controlled through a RS232 or USB interface?

The serial controlled DAT and ZX76 models (-SP & SN suffix) can be controlled via RS232 or USB using Mini-Circuits' "RS232 and USB to SPI convertor" models; RS232/USB-SPI or RS232/USB-SPI-N available from Mini-Circuits.

To control the parallel controlled DAT and ZX76 (PP & PN suffix models) via USB you can use USB I/O control boxes; USB-I/O-16D8R or USB-I/O-8DRV available from Mini-Circuits.

At this time there is no RS232 control option for the parallel controlled DAT and ZX76 models.

#### 32. What is the max control current?

For ZX76 series max control current is 400µA per control input of the attenuator when "1" logic signal applied.

The total maximum current for a parallel controlled 6 bit unit is  $400\mu$ A x 7 = 2.8mA (where "7" is 6 control signals + LE).

For a serial controlled ZX76 model the total control current is 400µA x 3 = 1.2mA (CLOCK+DATA+LE="3").

For the DAT models the max control current per control input is 1µA.

#### 33. When using a parallel control interface, do I need to be connected to a computer?

No, you can use a DIP switch & adjust the code manually for desired attenuation, or use computer control to set the values and then disconnect the control. As long as LE drops to '0' before the control values change the attenuation value will not change.

#### 34. Are there any changes in the performance of single and dual supply voltage attenuators when working with input frequencies close to DC?

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ISO 9001 ISO 14001 AS 9100 CEE



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Yes. In both types there is an expected performance drop.

Below 1MHz - IP3 degrades by 20 dB to 32dBm typ. Input power at 1 dB compression below 1MHz drops to about +15 to +20dBm typ vs. +24dBm at 0.2 dB typ. compression at input frequencies above1MHz.

35. In the DAT models, what is the purpose of the Latch Enable (LE) internal 100k $\Omega$  resistor to V<sub>DD</sub>?

The 100k $\Omega$  resistor is a pull-up resistor.

#### 36. What is the isolation between the RFin & RFout to the control lines?

FREQUANCY (MHz)	ATTENUATION (dB)	POWER OUT FOR RF OUT (dBm)	POWER OUT FOR PIN:3 (dBm)	ISOLATION (RF OUT - PIN:3) (dB)
500	0	-2.30	-33.14	-30.84
	0.5	-2.47	-32.67	-30.20
	1	-3.11	-32.40	-29.29
	2	-4.17	-32.42	-28.25
	4	-6.03	-31.93	-25.90
	8	-10.05	-32.63	-22.58
1000	0	-2.67	-17.26	-14.59
	0.5	-3.18	-17.18	-14.00
	1	-3.84	-17.58	-13.74
	2	-4.76	-17.81	-13.05
	4	-6.71	-17.69	-10.98
	8	-10.66	-18.18	-7.52

Please see the typical isolation summary table below:

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