# Mini-Circuits

# **MAR/RAM Kit Test Board Instructions for Use**

## (for testing all MAR-SM AND RAM models)

(AN-60-018)

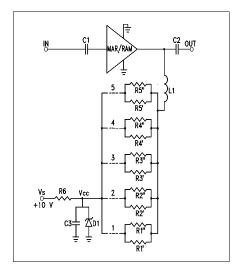
### Introduction

MAR-SM and RAM Models are series of amplifiers. They have different device voltages and currents (refer to catalog spec). The test board has been constructed in such a way as to make it useful for evaluating all the devices by suitable selection of bias resistor. This is done by soldering jumper wires across the dashed-lines positions 1 to 5 shown in Fig.1. The positions are defined in the table.

The Test Board has the following components	s:
---	----

Component	Value	Function	Model No.
C1 & C2	39000 pF	DC blocking	MAR-1SN RAM-1
L1	MCL Model # ADCH-80A	RF choke	MAR-2SN RAM-2
R1	288Ω	Sets bias current	MAR-3SN RAM-3
R2	196Ω	Sets bias current	MAR-4SN RAM-4
R3	89Ω	Sets bias current	MAR-6SN RAM-6
R4	402Ω	Sets bias current	MAR-7SM RAM-7
R5	268Ω	Sets bias current	MAR-8SM RAM-8
R6	4.75Ω	Protects Zener	MAR-8AS
D1	Zener, 10V	Protects against excessive supply voltage	
C3	0.1µF	Bypass capacitor; Bypass noise of supply voltage	

Fig 1. Schematic of the Test Board MAR/RAM - TB



MAR-1SM RAM-1	1
MAR-2SM RAM-2	2
MAR-3SM RAM-3	1,5
MAR-4SM RAM-4	3
MAR-6SM RAM-6	4
MAR-7SM RAM-7	5
MAR-8SM RAM-8	3,4,5
MAR-8ASM	1,4

Short at

#### Procedure

Follow these steps to use the Test Board. Figure 2 shows the layout.

- 1. Solder selected MAR-SM or RAM unit onto Test Board.
- Make DC connection by soldering jumper wire in accordance with the table, depending on the selected MAR-SM or RAM model. All other positions should be open.
- 3. Calibrate test setup.
- First, connect the RF output port of the test board to Network/Spectrum analyzer. Then, apply +10 V DC (10.2 V max). Finally, apply RF input to the test board from Network Analyzer.
- 5. Test Board has Insertion Loss due to the length of its lines, DC blocking capacitors and RF choke as shown below. Add this loss to the measured gain to get actual gain.

Frequency (GHz)	Insertion Loss (dB)
1	0.64
2	1.03
3	1.63
4	1.32
5	1.46
6	1.90
8	3.21

Fig 2. Layout of the Test Board MAR/RAM-TB

