



ESD Sensitivity Testing of Mini-Circuits ERA-4XSM (AN-60-028)

1.0 Purpose: To determine the Electrostatic Discharge Sensitivity of Mini-Circuits Amplifier ERA-4XSM in accordance with Human Body Model (HBM) and Machine Model (MM) ESD sensitivity standards. The failure criterion is: 1dB change in gain and/or 10% change in device voltage.

2.0 Ref.: ESD STM5.1-1993 (for HBM) and ESD STM5.2-1999 (for MM).

3.0 Human Body Model

Three (3) separate samples were used for each of the different values of ESD voltage: 150V, 200V, 240V, 499V, and 999V. Each sample was subjected to 3 ESD pulses of each polarity at each of 3 pairs of pins: input – output, input – ground, and output – ground, a total of 18 pulses.

Electrical performance testing was done for gain and DC device voltage at 65mA bias current, before and after the ESD pulses. Data are presented in Table 1. Using the failure criteria stated in 1.0, all devices passed at 499V; at 999V, 2 failed and 1 passed marginally.

4.0 Machine Model

4.1 Testing per ESD STM5.2-1999

Three (3) separate samples were used for each of the different values of ESD voltage: 50V, 100V, and 150V. Each sample was subjected to 3 ESD pulses of each polarity at each of 3 pairs of pins: input – output, input – ground, and output – ground, a total of 18 pulses.

Electrical performance testing was done for gain and DC device voltage at 65mA bias current, before and after the ESD pulses. Data are presented in Table 2. Using the failure criteria stated in 1.0, the devices passed at 50V and failed at 100V.

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Table 1 – Human Body Model

[150 v Human Body Model]													
Units		1				2				3			
Gain (dB)	Frequency	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change
	100	14.55	14.55	0		14.56	14.5	-0.06		14.57	14.54	-0.03	
	2000	13.44	13.64	0.2		13.44	13.5	0.06		13.42	13.48	0.06	
Vdd(v)	Idd=65mA	4.5	4.45	-0.05	-1.11%	4.5	4.45	-0.05	-1.11%	4.5	4.44	-0.06	-1.33%
[200 v HBM]													
Units		4				5				6			
Gain (dB)	Frequency	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change
	100	14.55	14.5	-0.05		14.56	14.51	-0.05		14.56	14.52	-0.04	
	2000	13.44	13.6	0.16		13.47	13.61	0.14		13.45	13.6	0.15	
Vdd(v)	Idd=65mA	4.5	4.45	-0.05	-1.11%	4.5	4.44	-0.06	-1.33%	4.5	4.45	-0.05	-1.11%
[240 v HBM]													
Units		7				8				9			
Gain (dB)	Frequency	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change
	100	14.55	14.51	-0.04		14.56	14.52	-0.04		14.56	14.52	-0.04	
	2000	13.45	13.52	0.07		13.43	13.74	0.31		13.45	13.66	0.21	
Vdd(v)	Idd=65mA	4.5	4.44	-0.06	-1.33%	4.5	4.44	-0.06	-1.33%	4.5	4.45	-0.05	-1.11%
[499 v HBM]													
Units		10				11				12			
Gain (dB)	Frequency	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change
	100	14.56	14.5	-0.06		14.56	14.5	-0.06		14.55	14.5	-0.05	
	2000	13.4	13.49	0.09		13.45	13.48	0.03		13.45	13.51	0.06	
Vdd(v)	Idd=65mA	4.5	4.47	-0.03	-0.67%	4.5	4.47	-0.03	-0.67%	4.5	4.47	-0.03	-0.67%
[999 v HBM]													
Units		25				26				27			
Gain (dB)	Frequency	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change
	100	14.56	-36.21	-50.77		14.55	0.96	-13.59		14.56	13.57	-0.99	
	2000	13.44	-9.8	-23.24		13.43	1.53	-11.9		13.45	12.51	-0.94	
Vdd(v)	Idd=65mA	4.5	3.33	-1.17	-26.00%	4.5	3.98	-0.52	-11.56%	4.5	4.35	-0.15	-3.33%

Table 2 – Machine Model

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[50 v Machine Model]		22				23				24			
Units													
Gain (dB)	Frequency	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change
	100	14.56	14.46	-0.1		14.55	14.53	-0.02		14.56	14.44	-0.12	
	2000	13.44	13.41	-0.03		13.43	13.46	0.03		13.45	13.39	-0.06	
Vdd(v)	Idd=65mA	4.5	4.5	0	0.00%	4.5	4.47	-0.03	-0.67%	4.5	4.5	0	0.00%
[100 v MM]		28				29				30			
Units													
Gain (dB)	Frequency	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change
	100	14.56	13.67	-0.89		14.6	13.63	-0.97		14.59	13.93	-0.66	
	2000	13.45	12.52	-0.93		13.49	12.54	-0.95		13.47	12.79	-0.68	
Vdd(v)	Idd=65mA	4.5	5.1	0.6	13.33%	4.53	5.14	0.61	13.47%	4.53	4.94	0.41	9.05%
[150 v MM]		13				14				15			
Units													
Gain (dB)	Frequency	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change	PRE-Test	POST-Test	DIF	% change
	100	14.56	-2.18	-16.74		14.56	-15.05	-29.61		14.56	-21.78	-36.34	
	2000	13.43	-2.86	-16.29		13.42	-13.06	-26.48		13.45	-20.64	-34.09	
Vdd(v)	Idd=65mA	4.5	3.4	-1.1	-24.44%	4.5	3.06	-1.44	-32.00%	4.5	2.42	-2.08	-46.22%

4.2 Additional Machine Model testing was done in three steps, to evaluate how much performance degradation occurs when progressively increasing ESD voltage is applied to a given device, and when a given ESD voltage is applied repeatedly with performance monitored after each pulse. Separate device samples were used for each of the three steps.

1. In Step 1, one ESD pulse of each polarity was applied with fixed amplitude of 100V to the different combinations of pins in order to determine the most sensitive pair of pins and most sensitive polarity. Purpose: to reduce the amount of testing required in the subsequent tests.
2. In Step 2, a sequence of ESD pulses was applied to each device at the most sensitive pair of pins and polarity found in Step 1, one pulse at each of the following voltages increasing in value: 50V, 70V, 100V, 150V, 200V. Gain and device voltage were measured initially and after each ESD pulse.
3. In Step 3, an ESD pulse with fixed amplitude of 100V was applied multiple times, at the most sensitive pair of pins and polarity found in Step 1, in order to determine cumulative effect of ESD stress.

Step 1 Test. Applying 100V ESD pulse showed the following: The most sensitive pin combination is input-to-ground where the “-” was applied to the input and “+” was applied to the ground. With that condition the gain dropped by 0.3dB and device voltage rose by 0.32V. The least sensitive pin combination is output-to-ground where the “+” was applied to the output and “-” was applied to the ground. With that condition the gain dropped by 0.08dB and device voltage rose by 0.02V. Table 3 lists the data.

Initial		After 100V Machine Model pulse		After 100V Machine Model pulse and previous pulse polarity	
	#1...#5	Input + , Ground -		Input - , Ground +	
	Gain, dB	Gain, dB		Gain, dB	
Avg	14.59	14.58		14.29	
Sigma	0.0075	0.0102		0.0377	
	Vdd, V	Vdd, V		Vdd, V	
Avg	4.48	4.48		4.80	
Sigma	0.0063	0.0040		0.0290	

	#6...#10	Output + , Ground -		Output - , Ground +	
	Gain, dB	Gain, dB		Gain, dB	
Avg	14.59	14.58		14.51	
Sigma	0.0098	0.0117		0.0075	
	Vdd, V	Vdd, V		Vdd, V	
Avg	4.47	4.47		4.49	
Sigma	0.0049	0.0089		0.0098	

	#11...#15	Output + , Input -		Output - , Input +	
	Gain, dB	Gain, dB		Gain, dB	
Avg	14.59	14.47		14.45	
Sigma	0.0080	0.0102		0.0242	
	Vdd, V	Vdd, V		Vdd, V	
Avg	4.47	4.71		4.72	
Sigma	0.0063	0.0117		0.0174	

Table 3 – “Step 1” Machine Model Test Data to Determine Most Sensitive Case

Step 2 Test. The results of progressively increasing the ESD stress, one pulse at each voltage, are shown in Figures 1 and 2.

Figure 1 - Gain vs ESD pulse voltage

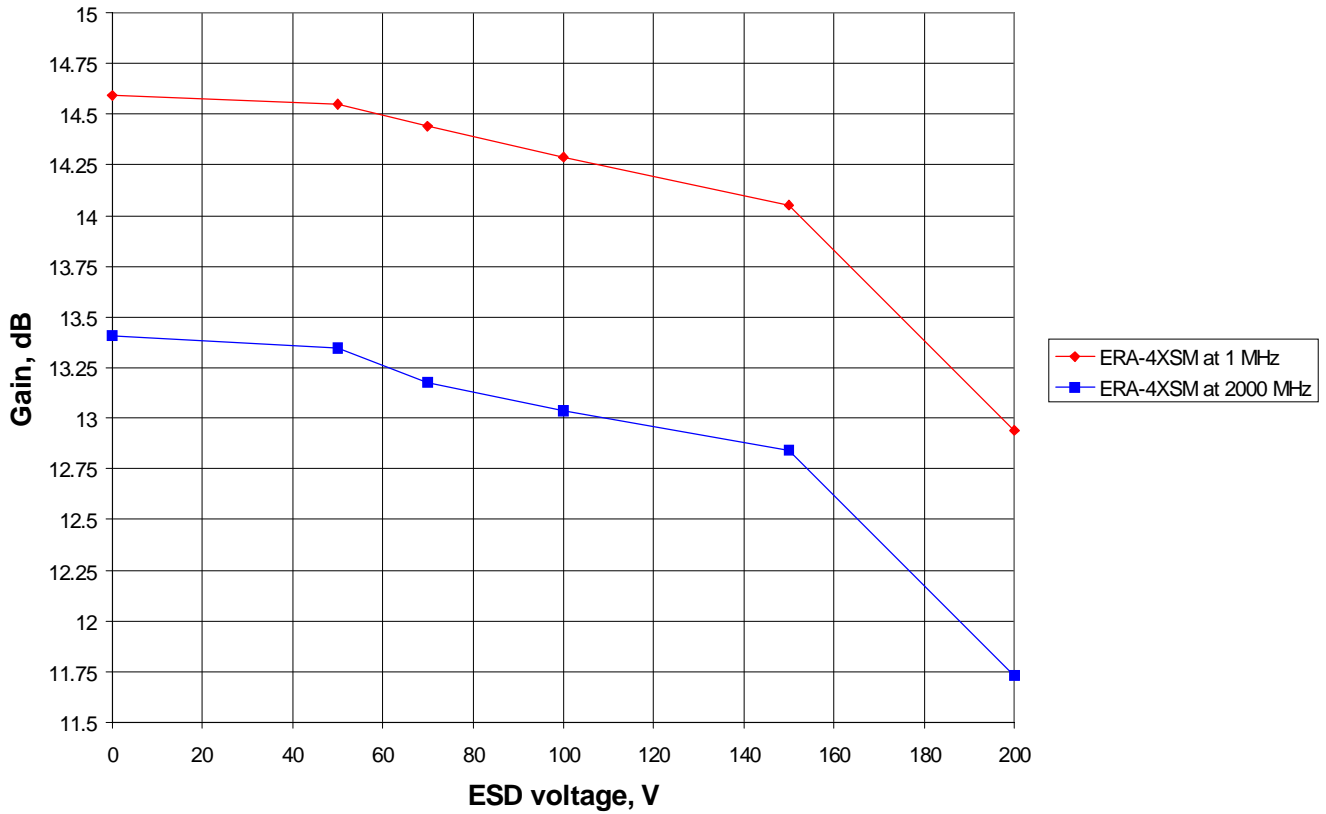
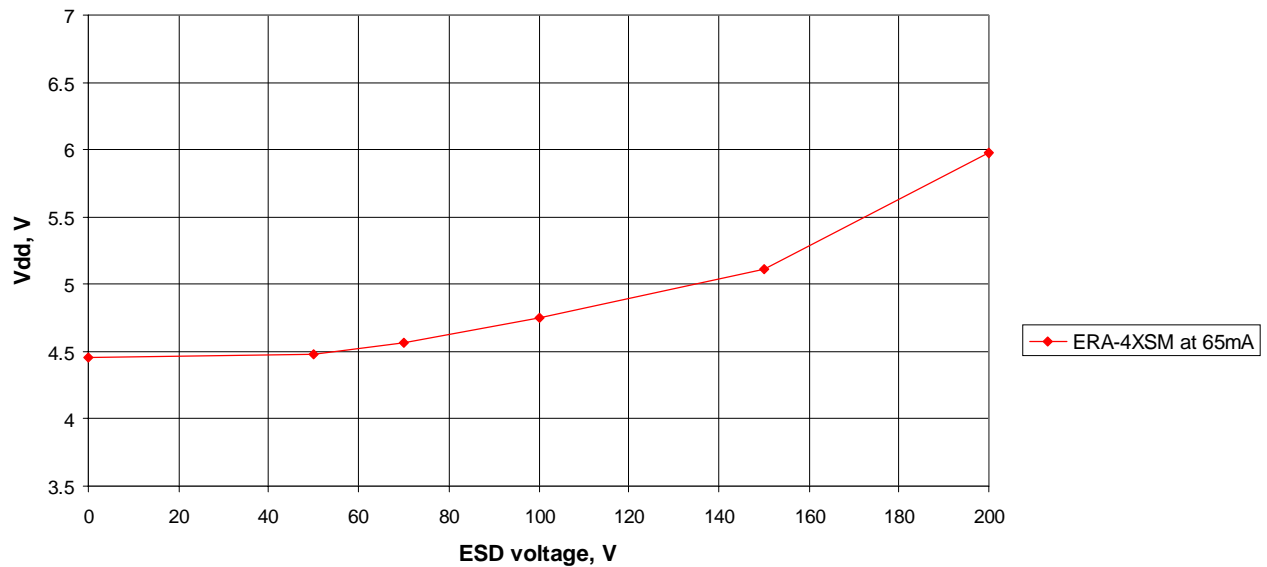


Figure 2 - Vdd vs ESD pulse voltage



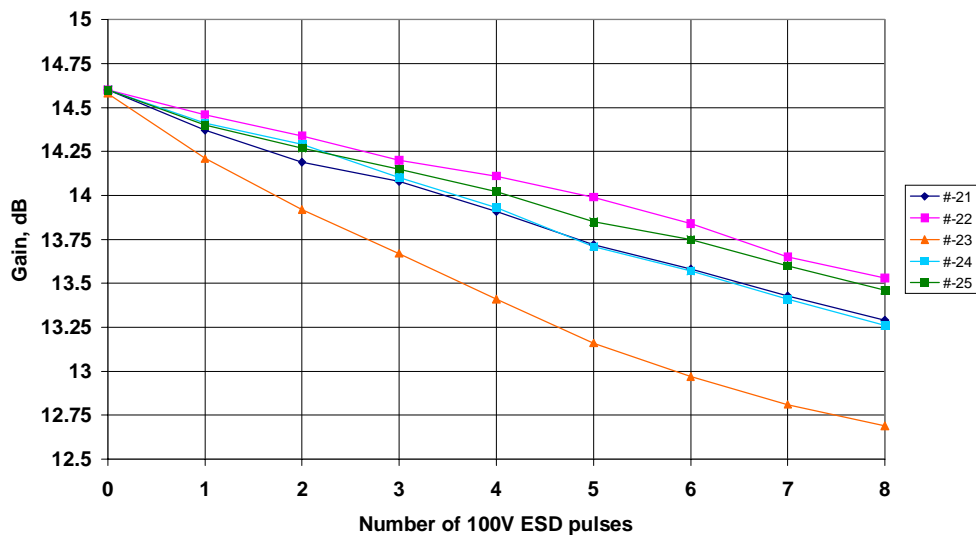
Figures 1 and 2 show that very little but still noticeable degradation in gain (0.1dB) and device voltage (0.1V) starts with the 70V ESD pulse.

At ESD pulse of 100V the changes in gain and device voltage are gradually increasing. The degradation caused by the 100V ESD pulse is in very good correlation with the Step 1 measurements that were performed on other samples of ERA-4XSM.

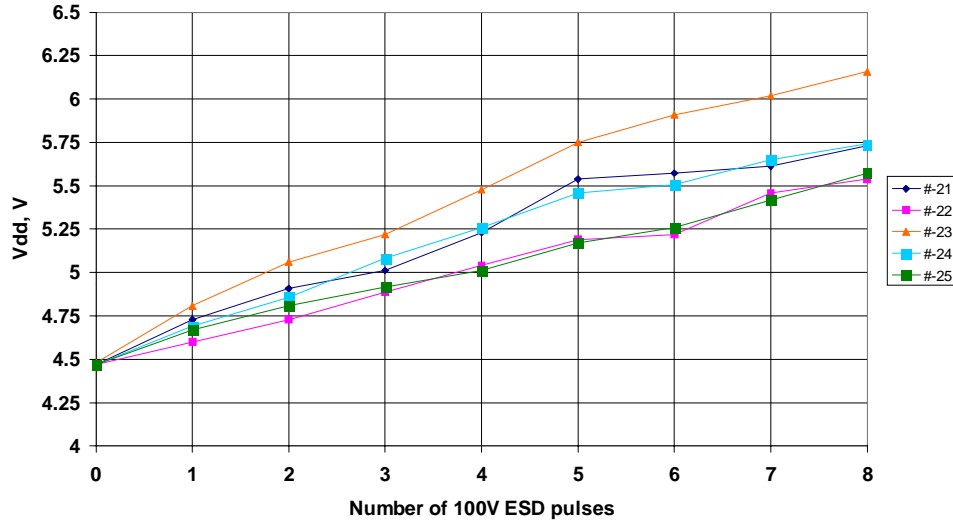
At ESD pulse of 150V more degradation is observed, but it is still gradual. This may be a cumulative effect rather than simply the effect of increased ESD voltage, as demonstrated by Step 3 (which was done with repeated 100V pulses).

Step 3 Test. Five units were stressed repeatedly with 100V ESD pulses. Electrical tests for gain and device voltage were made after each ESD pulse. The results are shown in Figures 3 and 4. After one pulse all 5 units passed the criteria of less than 1dB gain and less than 10% device voltage change. After 2 pulses, one failed the voltage criterion.

**Figure 3 - Gain at 1 MHz
vs. number of 100 V ESD pulses**



**Figure 4 - Vdd at 65mA
vs. number of 100 V ESD pulses**



5.0 Conclusions

5.1 Human Body Model:

The new amplifier ERA-4XSM can withstand ESD at least up to 499V (Class 1A).

5.2 Machine Model:

The new amplifier ERA-4XSM shows gradual degradation in the gain and the device voltage. That fact is not so bad. Even with the multiple stress a customer would rather have gradual changes than catastrophic failure. The amplifier withstands a single 100V ESD pulse, or 3 pulses at 50V.