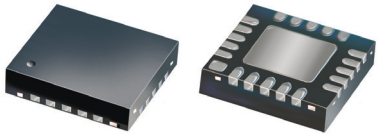
NON-CATALOG

Digital Step Attenuator 75Ω DC-2000 MHz

31 dB, 1dB Step
5 Bit, Parallel Control Interface, Dual Supply Voltage

Product Features
- Dual Supply Voltage: V_{DD}=+3V, V_{SS}=-3V
- Immune to latch up
- Excellent accuracy, 0.1 dB Typ
- Parallel control interface
- Fast switching control frequency, 1 MHz typ.
- Low Insertion Loss
- High IP3, +52 dBm
- Very low DC power consumption
- Excellent return loss, 20 dB Typ
- Small size 4.0 x 4.0 mm



DAT-3175-PN+
DAT-3175-PN

CASE STYLE: DG983-1

Typical Applications
- Base Station Infrastructure
- Portable Wireless
- CATV & DBS
- MMDS & Wireless LAN
- Wireless Local Loop
- UNII & Hiper LAN
- Power amplifier distortion canceling loops

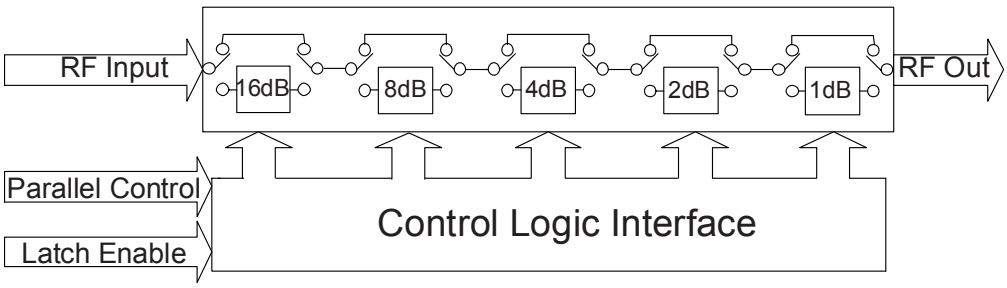
+RoHS Compliant
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

This model will be replaced in the future with a improved design. The new model will be DAT-3175A-PN+. It will have similar performance, the same case style and footprint.

General Description

The DAT-3175-PN is a 75Ω RF digital step attenuator that offers an attenuation range up to 31 dB in 1.0 dB steps. The control is a 5-bit parallel interface, operating on dual supply voltage: V_{DD}=+3V, V_{SS}=-3V. The DAT-3175-PN is produced using a unique CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Simplified Schematic



RF Electrical Specifications, DC-2000 MHz, T_{AMB}=25°C, V_{DD}=+3V, V_{SS}=-3V

Parameter	Freq. Range (GHz)	Min.	Typ.	Max.	Units
Accuracy @ **1 dB** Attenuation Setting	DC-1.2	—	0.03	0.24	dB
	1.2-2.0	—	0.1	0.25	dB
Accuracy @ **2 dB** Attenuation Setting	DC-1.2	—	0.07	0.28	dB
	1.2-2.0	—	0.15	0.3	dB
Accuracy @ **4 dB** Attenuation Setting	DC-1.2	—	0.05	0.36	dB
	1.2-2.0	—	0.15	0.4	dB
Accuracy @ **8 dB** Attenuation Setting	DC-1.2	—	0.1	0.52	dB
	1.2-2.0	—	0.24	0.6	dB
Accuracy @ **16 dB** Attenuation Setting	DC-1.2		0.23	0.84	dB
	1.2-2.0		0.8	1.0	dB
Insertion Loss (note 1) @ all attenuator set to 0dB	DC-1.2	—	1.2	1.8	dB
	1.2-2.0	—	1.6	2.1	dB
Input IP3 (note 2) (At Min. and Max. Attenuation)	DC-2.0	—	+52	—	dBm
Input Power @ 0.2dB Compression (note 2) (At Min. and Max. Attenuation)	DC-2.0	—	+24	—	dBm
VSWR	DC-1.2	—	1.6	2.0	—
	1.2-2.0	—	1.7	2.0	—

DC Electrical Specifications

Parameter	Min.	Typ.	Max.	Units
V_{DD}, Supply Voltage	2.7	3	3.3	V
V_{SS}, Supply Voltage	-3.3	-3	-2.7	V
I_{DD} (I_{SS}), Supply Current, quiescent (note 3)	—	—	100	μA
Control Input Low	—	—	0.3xV_{DD}	V
Control Input High	0.7xV_{DD}	—	—	V
Control Current	—	—	1	μA

Notes:
1. I. Loss values are de-embedded from test board Loss (test board's Insertion Loss: 0.10dB @100MHz, 0.40dB @1200MHz, 0.55dB @2000MHz, 0.75dB @4000MHz).
2. Input IP3 and 1dB compression degrades below 1 MHz.
3. During turn-on and transition between attenuation states, device may draw up to 2mA.

Switching Specifications

Parameter	Min.	Typ.	Max.	Units
Switching Speed, 50% Control to 0.5dB of Attenuation Value	—	1.0	—	μSec
Switching Control Frequency	—	1.0	—	MHz

Absolute Maximum Ratings

Parameter	Ratings
Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 100°C
V_{DD}	-0.3V Min., 4V Max.
V_{SS}	-4V Min., 0.3V Max.
Voltage on any input	-0.3V Min., V_{DD}+0.3V Max.
ESD, HBM	500V
ESD, MM	100V
Input Power	+24dBm

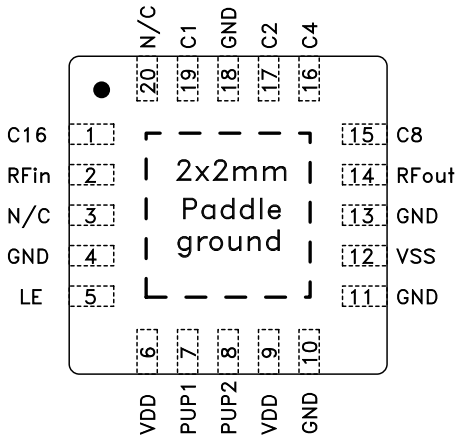
Permanent damage may occur if any of these limits are exceeded.

Pin Description

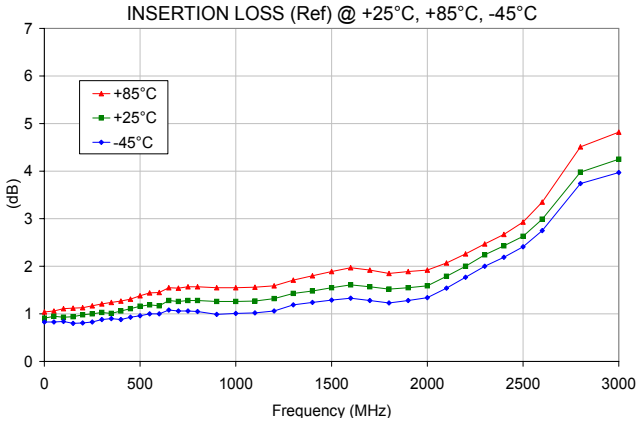
Function	Pin Number	Description
C16	1	Control for Attenuation bit, 16dB (Note 3)
RF in	2	RF in port (Note 1)
N/C	3	Not connected (Note 4)
GND	4	Ground connection
LE	5	Latch Enable Input (Note 2)
V_{DD}	6	Positive Supply Voltage
PUP1	7	Power-up selection
PUP2	8	Power-up selection
V_{DD}	9	Positive Supply Voltage
GND	10	Ground connection
GND	11	Ground connection
V_{SS}	12	Negative Supply Voltage
GND	13	Ground connection
RF out	14	RF out port (Note 1)
C8	15	Control for attenuation bit, 8 dB
C4	16	Control for attenuation bit, 4 dB
C2	17	Control for attenuation bit, 2 dB
GND	18	Ground Connection
C1	19	Control for attenuation bit, 1 dB
N/C	20	Not connected (Note 4)
GND	Paddle	Paddle ground (Note 5)

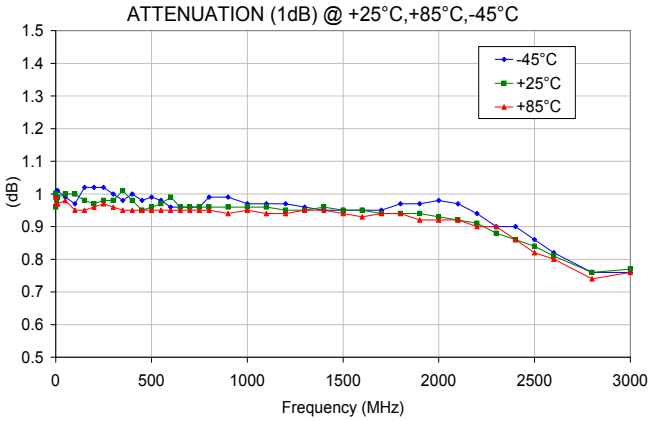
Notes:
1. Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.
2. Latch Enable (LE) has an internal 100KΩ resistor to V_{DD}.
3. Place a 10KΩ resistor in series, as close to pin as possible to avoid freq. resonance.
4. Place a shunt 10KΩ resistor to GND.
5. The exposed solder pad on the bottom of the package (See Pin configuration) must be grounded for proper device operation.

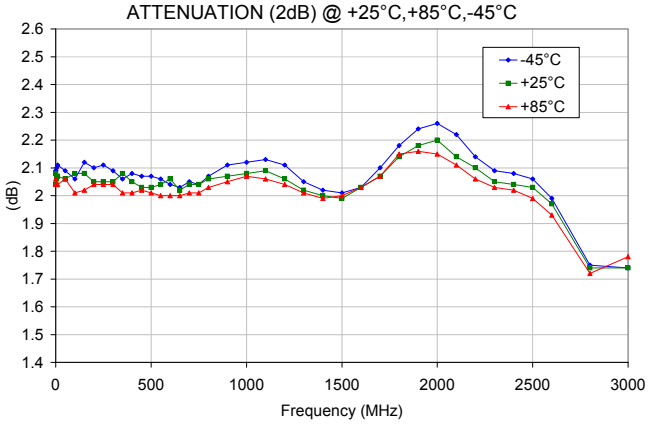
Pin Configuration (Top View)

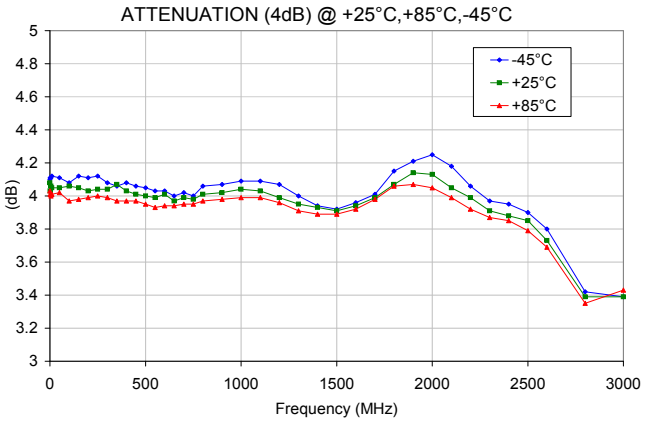


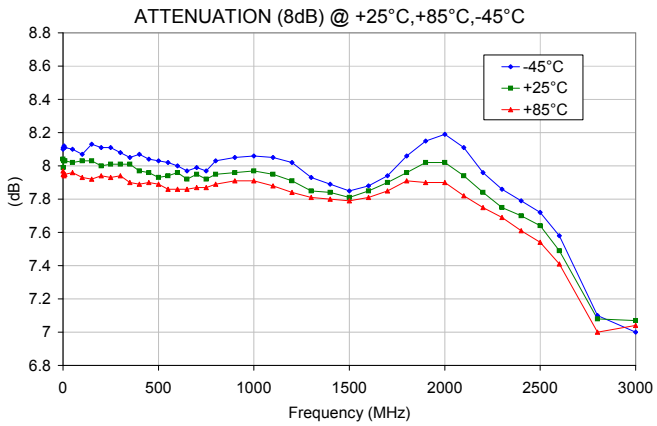
Typical Performance Curves

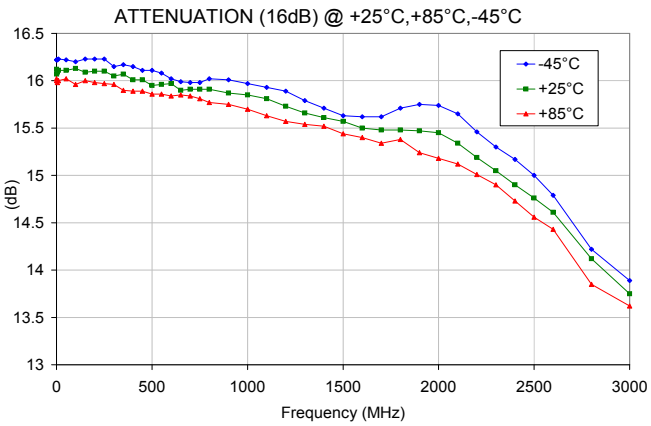












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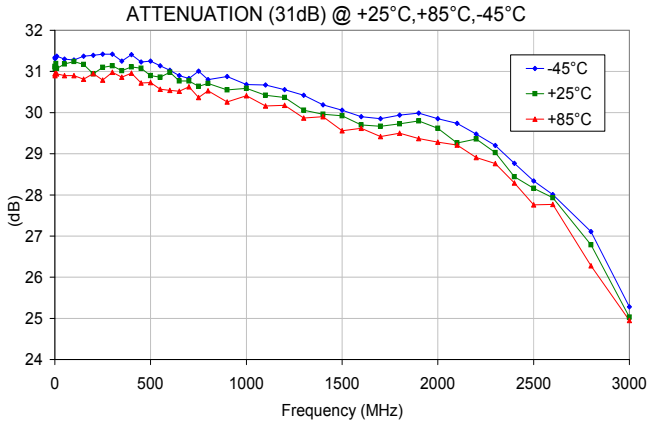
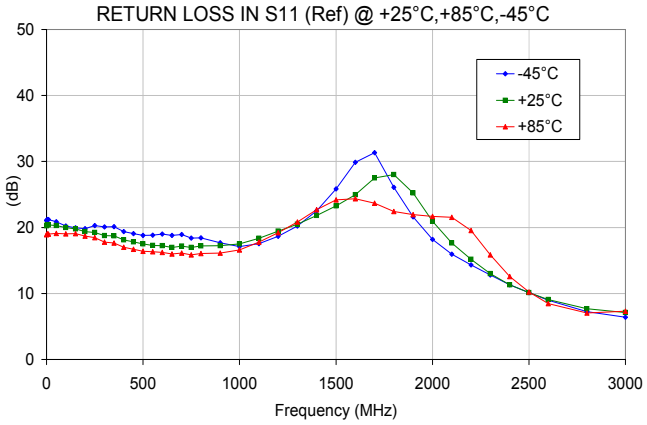
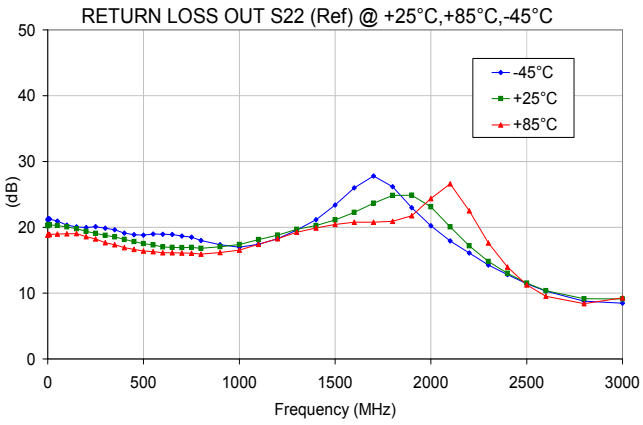
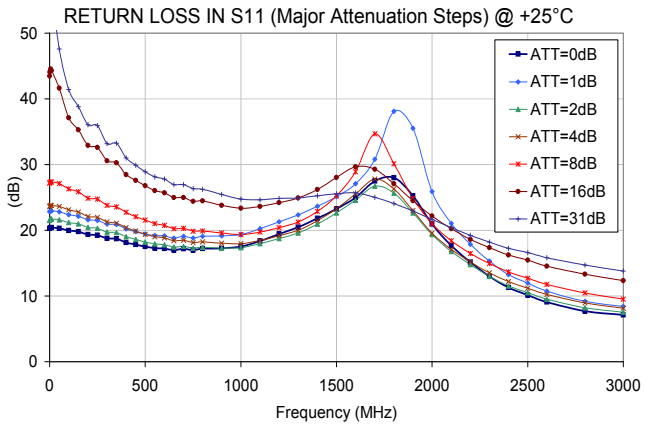
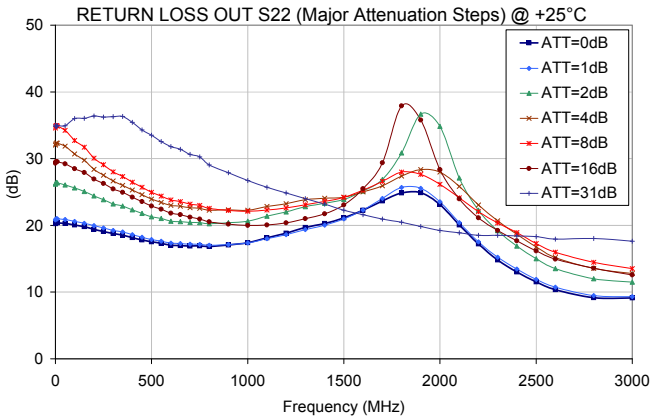


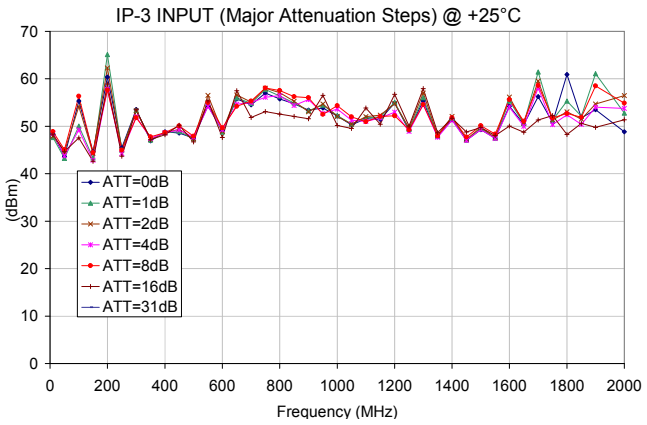


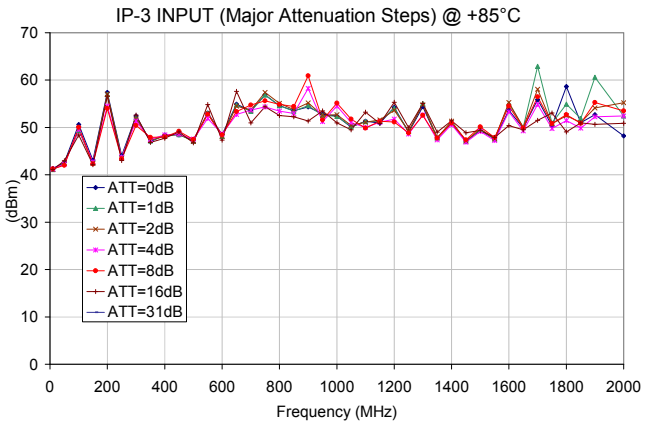


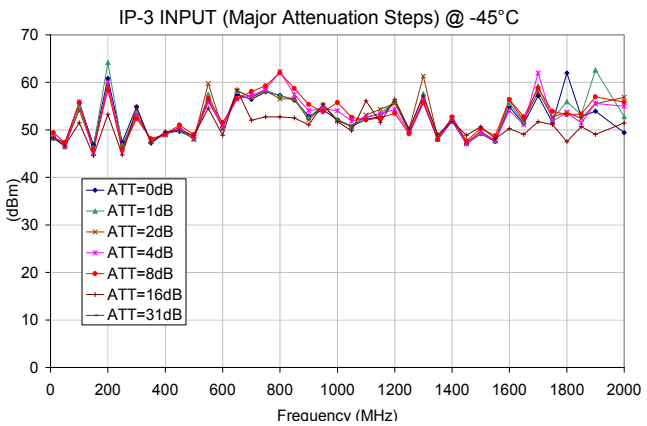


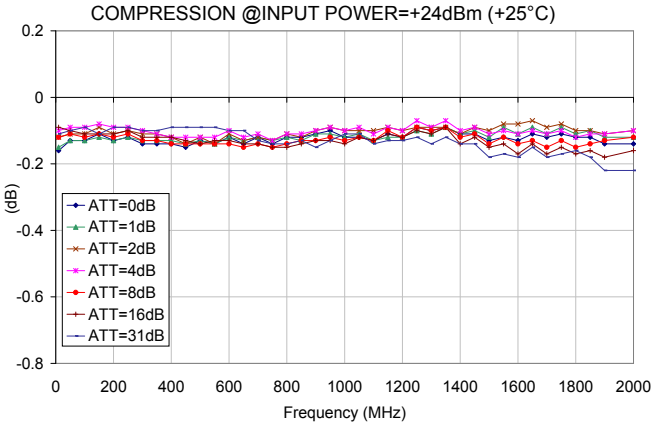


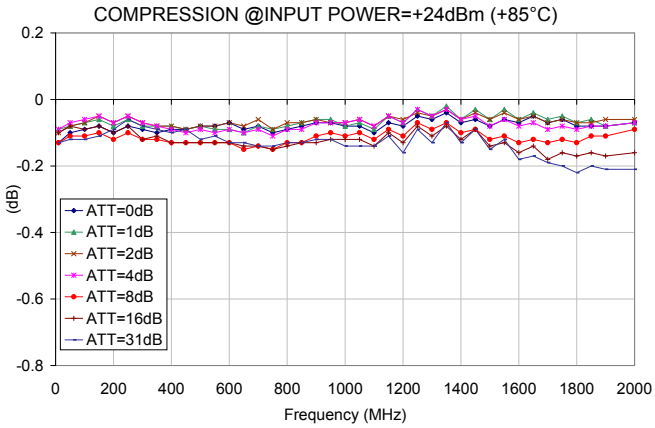
Typical Performance Curves

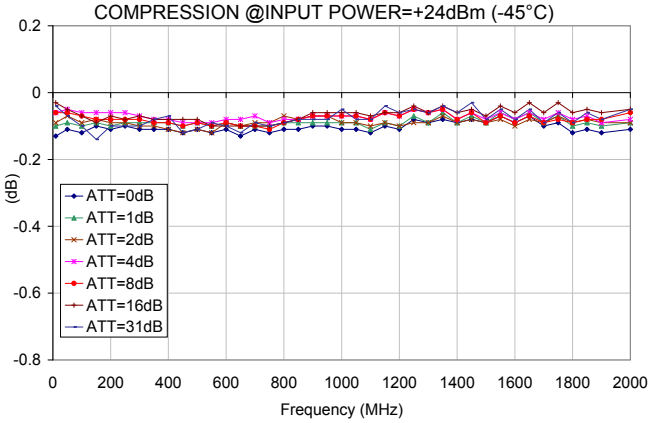




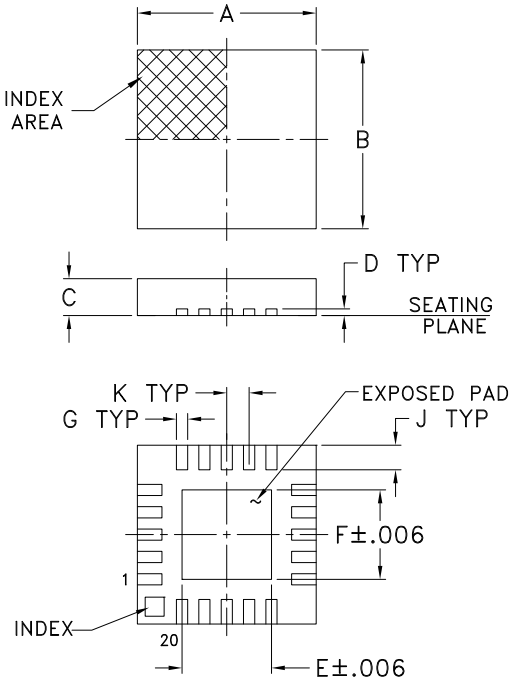




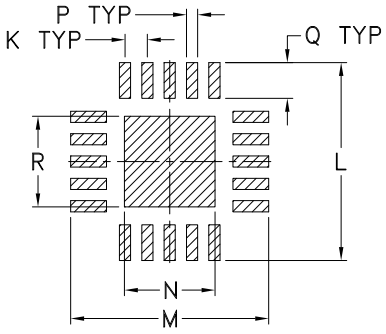




Outline Drawing (DG983-1)

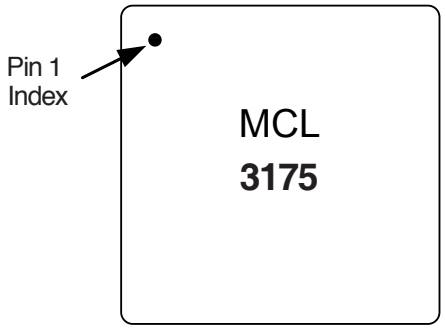


PCB Land Pattern



Suggested Layout,
Tolerance to be within ±.002

Device Marking

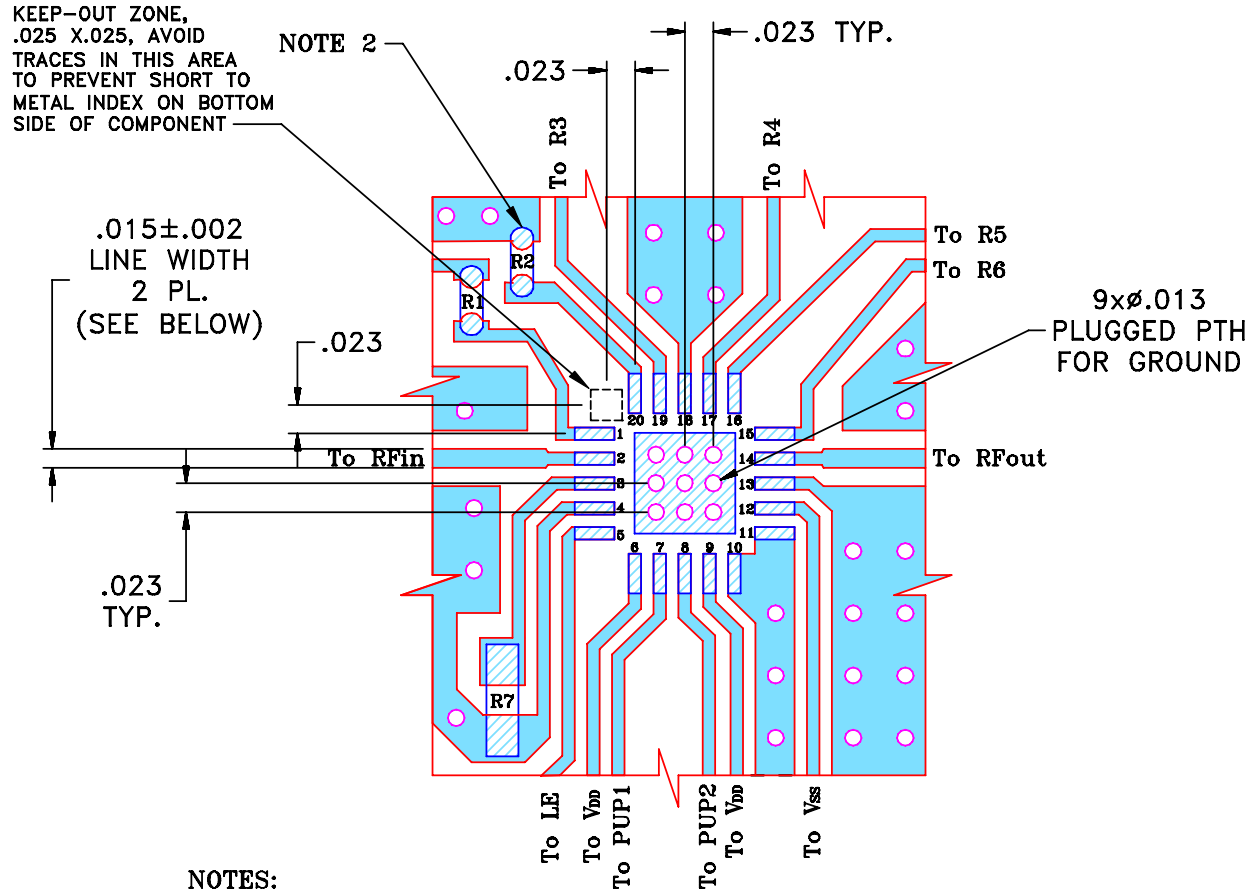


Outline Dimensions (inch/mm)

A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	WT. GRAMS
.157	**.157**	**.035**	**.008**	**.081**	**.081**	**.010**	**—**	**.022**	**.020**	**.177**	**.177**	**.081**	**.010**	**.032**	**.081**	.04
4.00	4.00	0.90	0.20	2.06	2.06	0.25	—	0.56	0.50	4.50	4.50	2.06	0.25	0.81	2.06	

Suggested Layout for PCB Design (PL-192)

The suggested Layout shows only the footprint area of the DAT, and the components located near this area (i.e.: R1, R2, R7). For the complete Layout, see photo and schematic diagram on page 11 of 12.



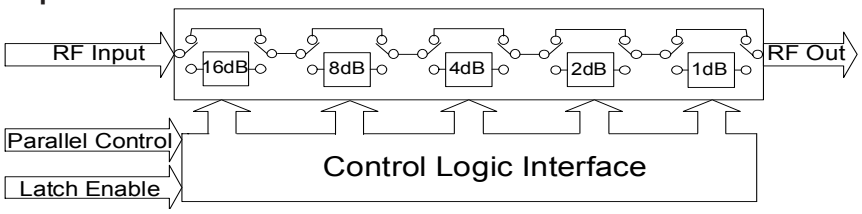
NOTES:

1. TRACE WIDTH IS SHOWN FOR FR4 WITH DIELECTRIC THICKNESS. .025"±.002". COPPER: 1/2 OZ. EACH SIDE. FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE MODIFIED.
2. 0603, 0402 SIZES CHIP FOOT PRINTS SHOWN FOR REFERENCE, VALUES OF RESISTORS WILL VARY BASED ON APPLICATION.
3. BOTTOM SIDE OF THE PCB IS CONTINUOUS GROUND PLANE.

DENOTES PCB COPPER LAYOUT WITH SMOBC (SOLDER MASK OVER BARE COPPER)

DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK

Simplified Schematic



The DAT-3175-PN parallel interface consists of 5 control bits that select the desired attenuation state, as shown in Table 1: Truth Table

Table 1. Truth Table

Attenuation State	C16	C8	C4	C2	C1
Reference	0	0	0	0	0
1 (dB)	0	0	0	0	1
2 (dB)	0	0	0	1	0
4 (dB)	0	0	1	0	0
8 (dB)	1	0	0	0	0
16 (dB)	1	0	0	0	0
31 (dB)	1	1	1	1	1
Note: Not all 32 possible combinations of C1 - C16 are shown in table					

The parallel interface timing requirements are defined by **Figure 1** (Parallel Interface Timing Diagram) and **Table 2** (Parallel Interface AC Characteristics), and switching speed.

For latched parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per Figure 1) to latch new attenuation state into device.

For direct parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Figure 1: Parallel Interface Timing Diagram

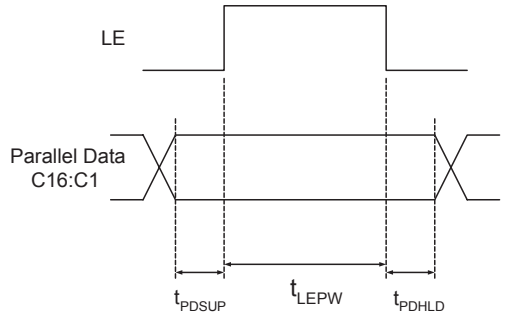


Table 2. Parallel Interface AC Characteristics

Symbol	Parameter	Min.	Max.	Units
t_{LEPW}	LE minimum pulse width	10		ns
t_{PDSUP}	Data set-up time before clock rising edge of LE	10		ns
t_{PDHLD}	Data hold time after clock falling edge of LE	10		ns

Pin 20 must always be low to prevent the attenuator from entering an unknown state.

Power-up Control Settings

The DAT-3175-PN always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial parallel control word is provided.

When the attenuator powers up with LE=0, the control bits are automatically set to one of four possible values. These four values are selected by the two power-up control bits, PUP1 and PUP2, as shown in Table 3: (Power-Up Truth Table, Parallel Mode)

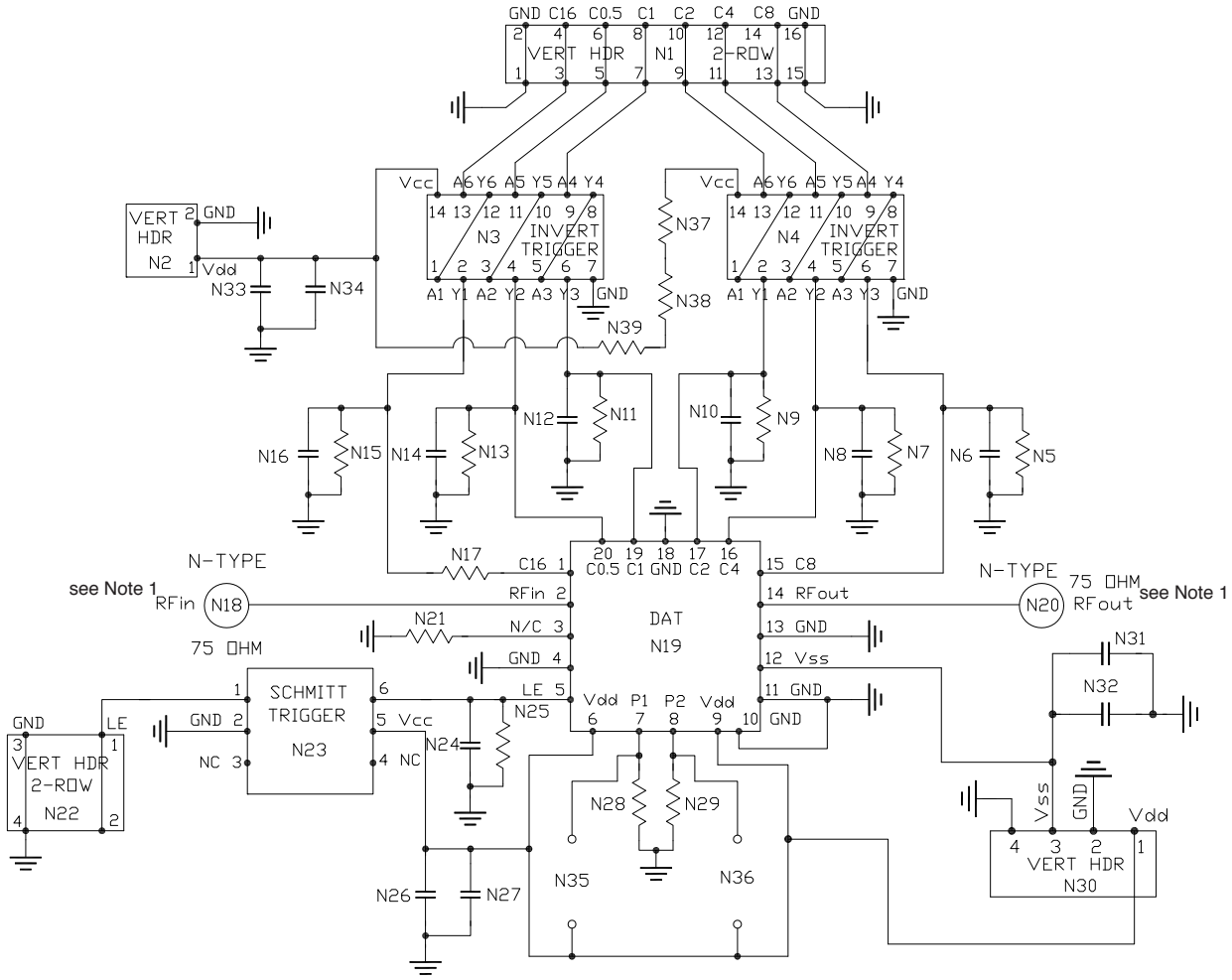
Table 3. Power-Up Truth Table, Parallel Mode

Attenuation State	PUP1	PUP2	LE
Reference	0	0	0
8 (dB)	0	1	0
16 (dB)	1	0	0
31 (dB)	1	1	0
Defined by C1-C16 (See Table 1-Truth Table)	X (Note 1)	X (Note 1)	1

Note: PUP1 and PUP2 Connection may be 0, 1, GROUND, or not connect, without effect on attenuation state.

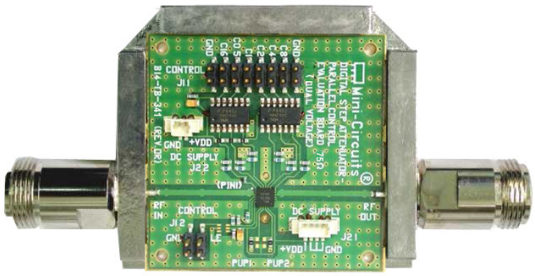
Power-Up with LE=1 provides normal parallel operation with C1-C16, and PUP1 and PUP2 are not active.

TB-341 Evaluation Board Schematic Diagram



Note 1: Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.

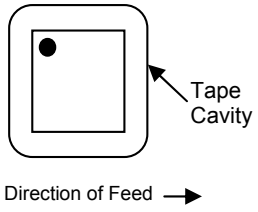
Bill of Materials	
N5, N7, N9, N11, N13, N15, N21 & N25	Resistor 0603 10 KOhm +/- 1%
N28 & N29	Resistor 0603 475 Ohm +/- 1%
N37-N39	Resistor 0603 0 Ohm
N17	Resistor 0402 10 KOhm +/- 1%
N6, N8, N10, N12, N14, N16, N24, N26, N31 & N33	NPO Capacitor 0603 100pF +/- 5%
N27, N32 & N34	Tantalum Capacitor 0805 100nF +/- 10%
N3 & N4	Hex Invert Schmitt Trigger MSL1
N23	Dual Schmitt Trigger Buffer SC-70 MSL1



TB-341

Tape and Reel Packaging Information

Table T&R

TR No.	No. of Devices	Reel Size	Tape Width	Pitch	Unit Orientation
F87	Small quantity standards 20, 50, 100, 200	7 inch	12 mm	8 mm	
	3000 (Standard)	13 inch			

Additional Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.

C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp