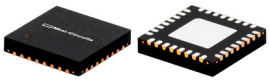
Digital Controlled Variable Gain Amplifier DVGA1-242A+

50Ω 0.45 to 2.4 GHz
31.5 dB, 0.5 dB Step, 6 Bit Serial Control

The Big Deal

- Integrated Amplifier and Digital Attenuator
- 30 dB Gain / 31.5 dB Gain Control
- High Output IP3, 35-37 dBm



CASE STYLE: DG1677

Product Overview

The DVGA1-242A+ is a 50Ω RF Digital Variable Gain Amplifier that offers an attenuation of 31.5 dB in 0.5 dB steps using a 6-bit serial interface attenuator and 30dB gain using a E-PHEMT amplifier. Step attenuator used in DVGA1-242A+ is produced using a unique combination of CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Key Features

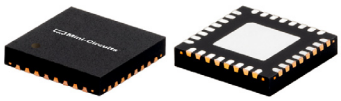
Feature	Advantages
31.5 dB attenuation in 0.5 dB step size	Combining high gain and a wide range of gain control makes the DVGA1-242A+ an ideal building block for any RF chain where level setting control is required in a small space.
High Gain, 30 dB	Incorporating multiple stages of amplification, the DVGA1-242A+ provides high gain reducing cost and PCB board space
High IP3, +35.1 dBm at 1.0 GHz Low Noise Figure, 2.2 dB at 1.0 GHz	Combining Low Noise and High IP3 makes this MMIC amplifier ideal for Low Noise Receiver Front End (RFE) giving the user advantages at both ends of the dynamic range: sensitivity & two-tone IM dynamic range.
Output Power, +22.7 dBm at 2.4 GHz	The DVGA1-242A+ maintains consistent output power capability over the full operating temperature range making it ideal to be used in remote applications such as LNB's as the L Band driver stage.
MCLP Package	Low Inductance, repeatable transitions, excellent thermal pad.
Max Input Power, +24 dBm	Ruggedized design operates up to input powers often seen at Receiver inputs.
Attenuation Step size, 0.5 dB, accuracy 0.1 dB typ. Total attenuation, 31.5 dB	Enables precise control of gain in 0.5 dB steps up to 31.5 dB.
External Jumper	Customer access is provided between the digital attenuator and the RF amplifier to allow the user to integrate external circuit elements if desired.

Digital Controlled Variable Gain Amplifier 50Ω 450-2400 MHz

30 dB Gain, 0.5 dB Step, 31.5 dB Attenuation,
6 Bit Serial Control

Product Features

- 31.5 dB Gain control 0.5dB step size
- Gain, 30 dB nominal at 0dB attenuation and 1 GHz
- Excellent accuracy, 0.1 dB typ
- Serial control interface
- Small size 5.0 x 5.0 mm



Generic photo used for illustration purposes only

CASE STYLE: DG1677

DVGA1-242A+

+RoHS Compliant
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Typical Applications

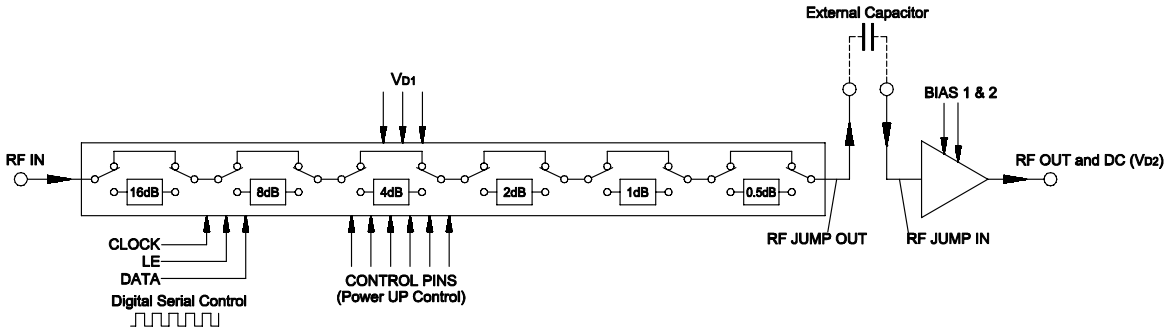
- Base Station Infrastructure
- GPS
- LTE
- WCDMA

General Description

The DVGA1-242A+ is a 50Ω RF Digital Variable Gain Amplifier that offers an attenuation of 31.5 dB in 0.5 dB steps using a 6-bit serial interface attenuator and 30dB gain using a E-PHEMT amplifier. Step attenuator used in DVGA1-242A+ is produced using a unique combination of CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Simplified Schematic

(Refer to Table 1 for Pad description)



RF Electrical Specifications[1] at 25°C, 50Ω With V_{D1}=+3.0V, V_{D2}=+5V

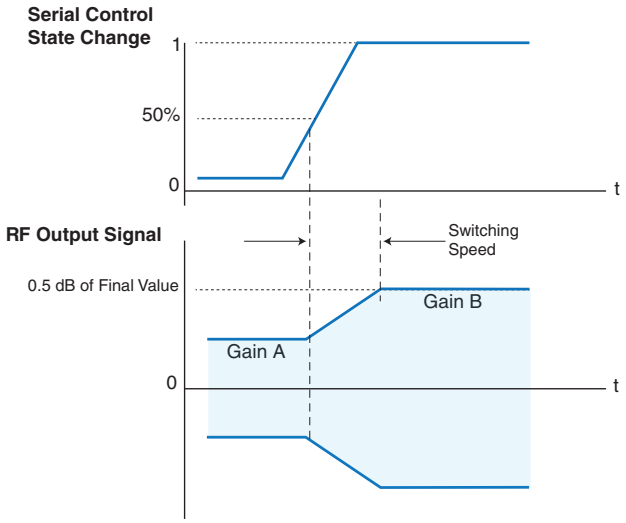
Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency Range		0.45		2.4	GHz
Gain (at 0 dB attenuation)	.45	—	29.6	—	dB
	1.0	—	30.5	—	
	1.4	26.5	29.3	32.4	
	2.0	—	24.3	—	
	2.4	—	21.0	—	
Input Return Loss (all states)	.45	—	17.3	—	dB
	1.0	—	20.2	—	
	1.4	—	7.6	—	
	2.0	—	7.7	—	
	2.4	—	11.4	—	
Output Return Loss (all states)	.45	—	21.0	—	dB
	1.0	—	13.4	—	
	1.4	—	12.1	—	
	2.0	—	9.8	—	
	2.4	—	9.9	—	
Output Power @ 1 dB compression (at min and max attenuation)	.45	—	22.1	—	dBm
	1.0	—	22.4	—	
	1.4	20.0	22.9	—	
	2.0	—	22.9	—	
	2.4	—	22.7	—	
Output IP3 (all states)	.45	—	35.7	—	dBm
	1.0	—	35.1	—	
	1.4	—	35.9	—	
	2.0	—	37.6	—	
	2.4	—	37.4	—	
Noise Figure (at 0 dB attenuation)	.45	—	2.2	—	dB
	1.0	—	2.2	—	
	1.4	—	2.4	3.7	
	2.0	—	2.6	—	
	2.4	—	2.9	—	
Accuracy @ **0.5 dB** Attenuation Setting	.45 - 1.0	—	0.03	0.12	dB
	1.0 - 2.4	—	0.1	0.18	
Accuracy @ **1 dB** Attenuation Setting	.45 - 1.0	—	0.05	0.13	dB
	1.0 - 2.4	—	0.15	0.2	
Accuracy @ **2 dB** Attenuation Setting	.45 - 1.0	—	0.06	0.25	dB
	1.0 - 2.4	—	0.24	0.37	
Accuracy @ **4 dB** Attenuation Setting	.45 - 1.0	—	0.09	0.37	dB
	1.0 - 2.4	—	0.31	0.45	
Accuracy @ **8 dB** Attenuation Setting	.45 - 1.0	—	0.2	0.4	dB
	1.0 - 2.4	—	0.49	0.7	
Accuracy @ **16 dB** Attenuation Setting	.45 - 1.0	—	0.2	0.6	dB
	1.0 - 2.4	—	0.73	1.2	

1. Measured in Mini-Circuits characterization test board TB-643A+. See characterization Test Circuit (Fig. 2)

Attenuation Switching Specifications

Parameter	Min.	Typ.	Max.	Units
Switching Speed, 50% Control to 0.5dB of Attenuation Value	—	1.0	—	µSec
Switching Rep Rate	—	—	25	KHz

Figure 1. Switching Speed



DC Electrical Specifications

Parameter	Min.	Typ.	Max.	Units
Supply Voltage, V_{D1}	2.7	3.0	3.3	V
V_{D2}	4.75	5.0	5.25	V
Supply Current, I_{D1}	—	—	200	µA
I_{D2}	—	154	186	mA
Control Input Low	-0.3	—	0.6	V
Control Input High	1.17	—	3.6	V
Control Current*	—	—	20	µA

* Except 30 µA typ. for C 0.5, C16

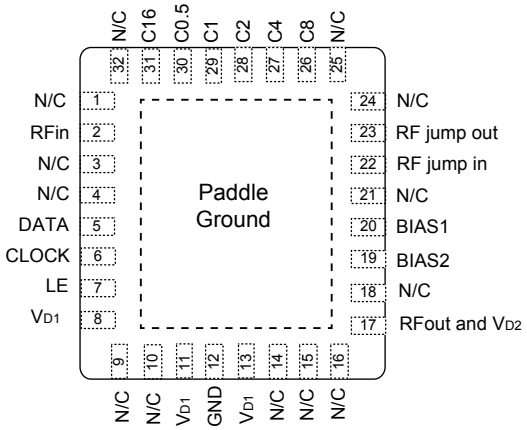
Absolute Maximum Ratings

Parameter	Ratings
Operating Temperature	-40°C to 85°C
Storage Temperature	-65°C to 150°C
V_{D1}	-0.3V Min., 5.5V Max.
V_{D2}	6.0V
Voltage on any control input**	-0.3V Min., V_{D1}+0.3V Max.
Input Power	+24dBm

** Permanent damage may occur if any of these limits are exceeded.

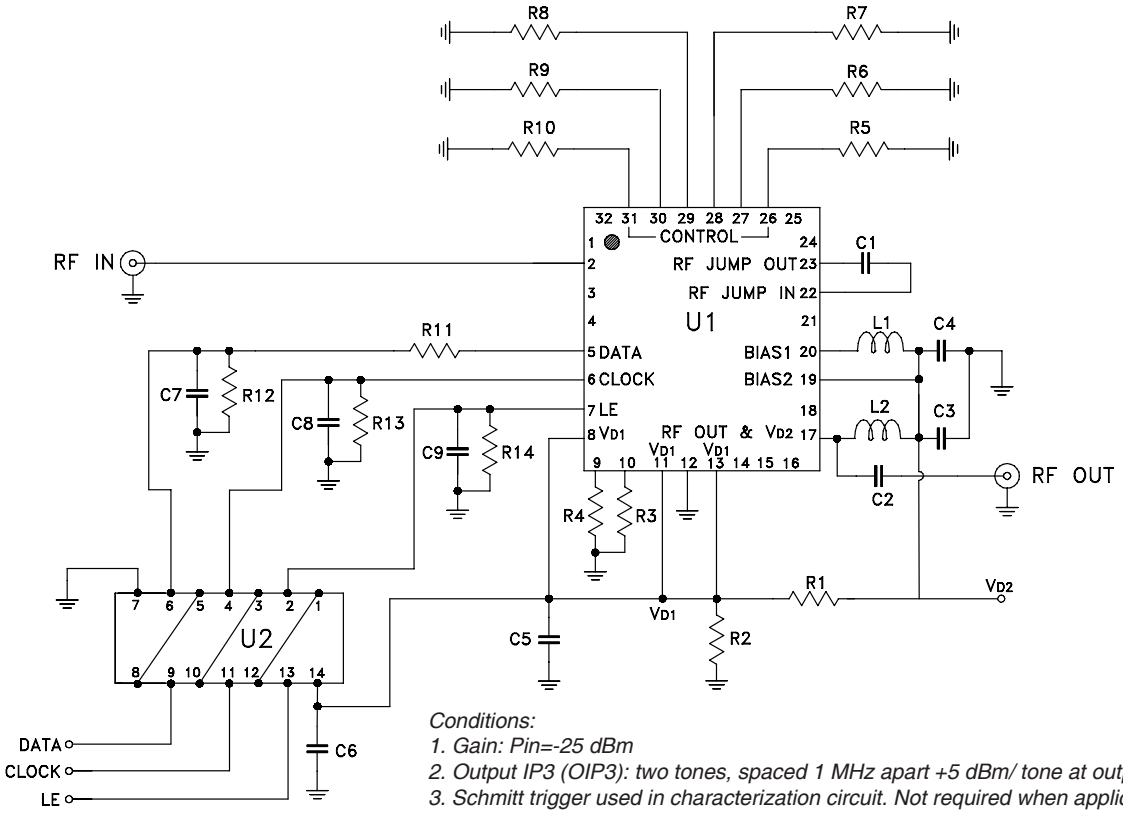
Table 1. Pad Description

Pin Number	Function	Description
1	N/C	Not Connected
2	RF IN	RF Input Port (Note 1)
3	N/C	Not Connected
4	N/C	Not Connected
5	DATA	Serial Interface Data Input (Note 3)
6	CLOCK	Serial Interface Clock Input
7	LE	Latch Enable Input (Note 2)
8	V_{D1}	V_{D1} Power Supply Input
9	N/C	Not Connected
10	N/C	Not Connected
11	V_{D1}	V_{D1} Power Supply Input
12	GND	Ground
13	V_{D1}	V_{D1} Power Supply Input
14	N/C	Not Connected
15	N/C	Not Connected
16	N/C	Not Connected
17	RF OUT &V_{D2}	RF output and V_{D2} on same pad (external Bias Tee) (Note1,6)
18	N/C	Not Connected
19	BIAS 2	Amplifier Bias 2 connects to V_{D2}
20	BIAS 1	Amplifier Bias 1 connects to V_{D2} via inductor(Note1,6)
21	N/C	Not Connected
22	RF JUMP IN	Interstage RF Jumper Input (Note 1)
23	RF JUMP OUT	Interstage RF Jumper Output (Note 1)
24	N/C	Not Connected
25	N/C	Not Connected
26	C8	Power Up Control for 8dB Att. Bit (Note 4)
27	C4	Power Up Control for 4dB Att. Bit (Note 4)
28	C2	Power Up Control for 2dB Att. Bit (Note 4)
29	C1	Power Up Control for 1dB Att. Bit (Note 4)
30	C0.5	Power Up Control for 0.5dB Att. Bit (Note 4)
31	C16	Power Up Control for 16dB Att. Bit (Note 4)
32	N/C	Not Connected
PADDLE	GND	Ground (Note5)



Notes:
1. All RF input and output ports shall be AC coupled with external blocking capacitor.
2. Latch Enable (LE) has an internal 100KΩ pull-up resistor to V_{D1}
3. Place a 10KΩ resistor in series, as close to pin as possible to avoid freq. resonance (see layout drawing PL-355).
4. Refer to Power-up Control Settings.
5. The exposed solder pad on the bottom of the package (See Pin Configuration) must be grounded for proper device operation
6. See application and characterization test circuit and layout drawing PL-355.

Application and Characterization Test Circuit



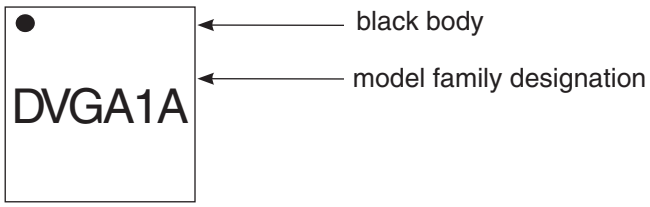
Conditions:
1. Gain: Pin=-25 dBm
2. Output IP3 (OIP3): two tones, spaced 1 MHz apart +5 dBm/ tone at output.
3. Schmitt trigger used in characterization circuit. Not required when application circuit includes recommended level settings.

Figure 2. Schematic of Test Circuit used for Characterization. (DUT soldered on Mini-Circuits Characterization Test Board TB-643A+). Gain, output power at 1 dB compression (P1dB) Output IP3 (OIP3), Noise Figure are measured using Agilent's N5242A PNA-X Microwave Network Analyzer.

Bill of Materials

Ref. Des.	Value / Description	Case Style, Size
C1, C4	100pF	0402
C2	100pF	0805
C3	1uF	0805
C5, C7, C8, C9	100pF	0603
C6	0.47uF	0805
L1	36nH	0402
L2	47nH	0402
R1	475Ω	0603
R2	681Ω	0603
R3 ~ R14	10kΩ	0603
U2	HEX Inverter Trigger Fairchild P/N MM74HC14M	
U1	DVGA1-242A+	

Product Marking



Simplified Schematic

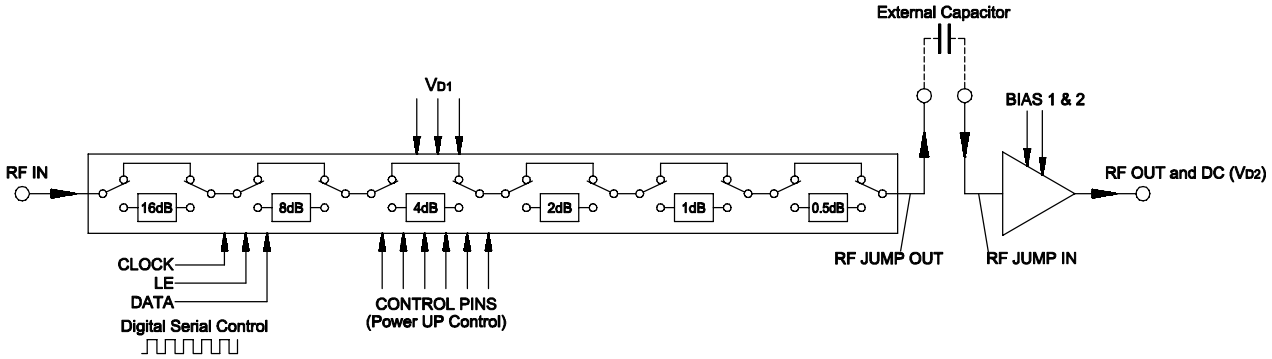


Figure 3. The DVGA1-242A+ Serial interface consists of 6 control bits that select the desired attenuation state, as shown in Table 2 Truth Table.

Table 2. Truth Table

Attenuation State	C16	C8	C4	C2	C1	C0.5
Reference	0	0	0	0	0	0
0.5 (dB)	0	0	0	0	0	1
1 (dB)	0	0	0	0	1	0
2 (dB)	0	0	0	1	0	0
4 (dB)	0	0	1	0	0	0
8 (dB)	0	1	0	0	0	0
16 (dB)	1	0	0	0	0	0
31.5 (dB)	1	1	1	1	1	1
Note: Not all 64 possible combinations of C0.5 - C16 are shown in table						

The serial interface is a 6-bit serial in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input. The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched. The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by Figure 4 (Serial Interface Timing Diagram) and Table 3 (Serial Interface AC Characteristics).

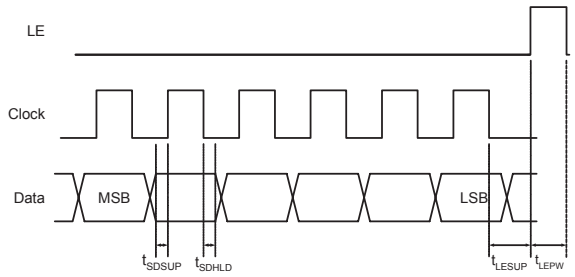


Figure 4. Serial Interface Timing Diagram

Table 3. Serial Interface AC Characteristics (V_{D1}=3V)

Symbol	Parameter	Min.	Max.	Units
f_{clk}	Serial data clock frequency (Note 1)		10	MHz
t_{clkH}	Serial clock HIGH time	30		ns
t_{clkL}	Serial clock LOW time	30		ns
t_{LESUP}	LE set-up time after last clock falling edge	10		ns
t_{LEPW}	LE minimum pulse width	30		ns
t_{SDSUP}	Serial data set-up time before clock rising edge	10		ns
t_{SDHLD}	Serial data hold time after clock falling edge	10		ns

Note 1. fclk verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10MHz to verify fclk specification.

The DVGA1-242A+, uses a common 6-bit serial, as shown in Table 4: 6-Bit attenuator Serial Programming Register Map. The first bit, the MSB, corresponds to the 16-dB Step and the last bit, the LSB, corresponds to the 0.5dB step.

Table 4. 6-Bit attenuator Serial Programming Register Map

B5	B4	B3	B2	B1	B0
C16	C8	C4	C2	C1	C0.5

MSB (first in) — LSB (last in)

Power-up Control Settings

The DVGA1-242A+ always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial serial control word is provided. When the attenuator powers up, the six control bits are set to whatever data is present on the six control inputs (C0.5 to C16). This allows any one of the 64 attenuation settings to be specified as the power-up state.

Additional Detailed Technical Information *additional information is available on our dash board. To access this information click here*	
Performance Data	Data Table
	Swept Graphs
	S-Parameter (S2P Files) Data Set (.zip file)
Case Style	DG1677 *Plastic package, exposed paddle, lead finish: Ni/Pd/Au*
Tape & Reel **Standard quantities available on reel**	F68 *7" reels with 20,50,100,200, 500 or 1K devices*
Suggested Layout for PCB Design	PL-355
Evaluation Board	TB-643A+
Environmental Ratings	ENV66

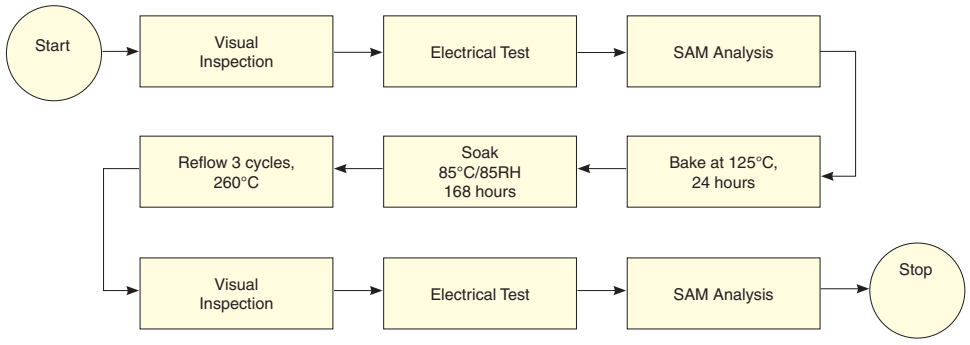
ESD Rating

Human Body Model (HBM): Class 1A (250 to <500V) in accordance with ANSI/ESD STM 5.1 - 2001
Machine Model (MM): Class M1 (40V) in accordance with ANSI/ESD STM5.2-1999

MSL Rating

Moisture Sensitivity: MSL1 in accordance with IPC/JEDEC J-STD-020D

MSL Test Flow Chart



Additional Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.

C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp