DOCSIS 3.1

Power Doubler Hybrid Module ADCA3950

75Ω 45 to 1218 MHz

FEATURES

Total composite power: 74 dBmV
High power gain: 25.0 dB at 1218 MHz
Excellent linearity
Very low distortion
- **Composite triple beat: –80 dBc typical**
- **Composite second-order: –78 dBc typical**
- **Carrier to intermodulation noise: 58 dB typical**

Low noise figure: 3 dB at 45 MHz and 4 dB at 1218 MHz
Unconditionally stable
Transient and surge protection

APPLICATIONS

45 MHz to 1218 MHz community access television (CATV) infrastructure amplifier systems
Remote physical layer (PHY)
DOCSIS 3.1 compliant

GENERAL DESCRIPTION

The Mini-Circuits' ADCA3950 is a power doubler hybrid module packaged in the industry-standard SOT-115J package. The device achieves a high RF output of 74 dBmV total composite power under 18 dB tilt conditions by using advanced circuit design techniques with gallium arsenide (GaAs), pseudomorphic high electron transistor (pHEMT), and gallium nitride (GaN) HEMT technologies. The ADCA3950 provides high gain, simplifying the design and manufacturing of DOCSIS 3.1™ infrastructure equipment.

This part was acquired by Mini-Circuits from Analog Devices on April 12, 2024.

FUNCTIONAL BLOCK DIAGRAM

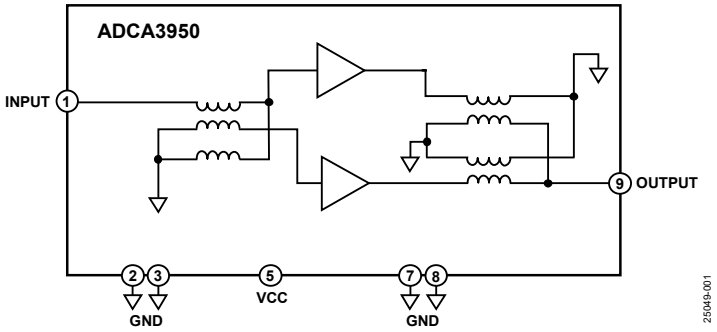

Figure 1.

REV. A
ECO-021744
ADCA3950
MCL NY
240508

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REVISION HISTORY

4/2024 - Revision A: Transferred from Analog Devices to Mini-Circuits

12/2020—Revision 0: Initial Version

SPECIFICATIONS

GENERAL PERFORMANCE

Supply voltage (V_{CC}) = 24 V, flange temperature (T_{FLANGE}) = 35°C, and source impedance (Z_S) = load impedance (Z_L) = 75 Ω, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER GAIN	S21		23.5		dB	Frequency = 45 MHz
			25.0		dB	Frequency = 1218 MHz
SLOPE STRAIGHT LINE[1]			1.0		dB	Frequency = 45 MHz to 1218 MHz
FLATNESS OF FREQUENCY RESPONSE[2]			0.6		dB	Frequency = 45 MHz to 1218 MHz
REVERSE ISOLATION	S12		−28		dB	Frequency = 45 MHz to 1218 MHz
RETURN LOSS						See Figure 3 and Figure 6
Input	S11		−20		dB	Frequency = 45 MHz to 320 MHz
			−18		dB	Frequency = 320 MHz to 640 MHz
			−18		dB	Frequency = 640 MHz to 870 MHz
			−18		dB	Frequency = 870 MHz to 1000 MHz
			−16		dB	Frequency = 1000 MHz to 1218 MHz
Output	S22		−20		dB	Frequency = 45 MHz to 320 MHz
			−20		dB	Frequency = 320 MHz to 640 MHz
			−20		dB	Frequency = 640 MHz to 870 MHz
			−20		dB	Frequency = 870 MHz to 1000 MHz
			−18		dB	Frequency = 1000 MHz to 1218 MHz
NOISE FIGURE			3		dB	Frequency = 45 MHz
			4		dB	Frequency = 1218 MHz
SUPPLY						
Operating Voltage	V_{CC}		24	26	V	
DC Current (Total)	$I_{CC\ (TOTAL)}$		470	490	mA	

[1] Slope straight line is defined as the delta between the gain at the start frequency and the gain at the stop frequency.
[2] Flatness of frequency response is defined as the delta between the gain at any frequency between the start and stop frequencies and a straight line reference drawn between the gain at the start frequency and the gain at the stop frequency.

DISTORTION DATA (ALL DIGITAL CHANNEL PLAN)

V_{CC} = 24 V, T_{FLANGE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
TOTAL COMPOSITE POWER	TCP		74		dBmV	18 dB tilt, 190 digital (256 QAMs) channels from 57 MHz to 1215 MHz
ERROR RATES						
Modulation Error Rate	MER		47		dB	
Bit Error Rate	BER		$<1 \times 10^{-10}$			Post Viterbi

DISTORTION DATA (MIXED SIGNAL CHANNEL PLAN)

V_{CC} = 24 V, T_{FLANGE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DISTORTION						TCP = 72.4 dBmV, the analog and digital channel plan consists of 18 dB extrapolated tilt, 79 continuous wave channels plus 111 digital channels, a National Television System Committee (NTSC) frequency raster range of 55.25 MHz to 547.25 MHz, and −6 dB offset
Composite Triple Beat	CTB		−80		dBc	Defined by the National Cable and Telecommunications Association (NCTA)
Composite Second-Order	CSO		−78		dBc	Defined by NCTA
Carrier to Intermodulation Noise			58		dB	Defined by American National Standard/Society of Cable Telecommunications Engineers (ANSI/SCTE) 17 (test procedure for carrier to noise)

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{CC}	
DC Supply over Voltage (5 Minute)	30 V
RF Input Voltage (RF_{INPUT}), Single Tone	75 dBmV
Operating Temperature Range	
T_A	−30°C to +85°C
T_{FLANGE}	−30°C to +100°C
Storage Temperature (T_S) Range	−40°C to +100°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

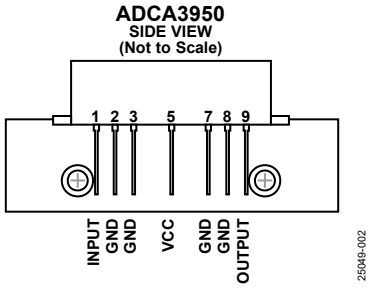

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INPUT	RF Input
2, 3	GND	Ground
5	VCC	Positive Supply Voltage, 24 V Typical
7, 8	GND	Ground
9	OUTPUT	RF Output

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 24 V, T_{FLANGE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

S-PARAMETERS

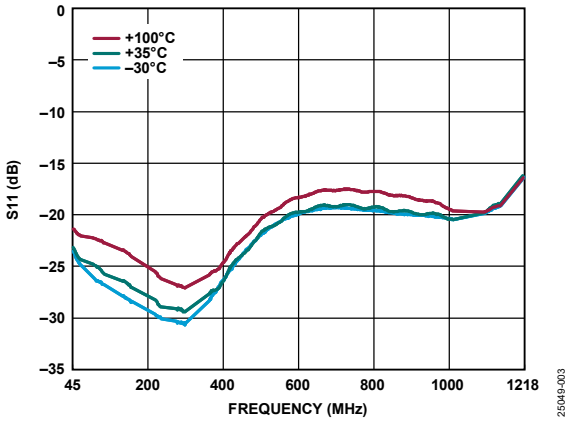

Figure 3. S11 vs. Frequency at Various Temperatures

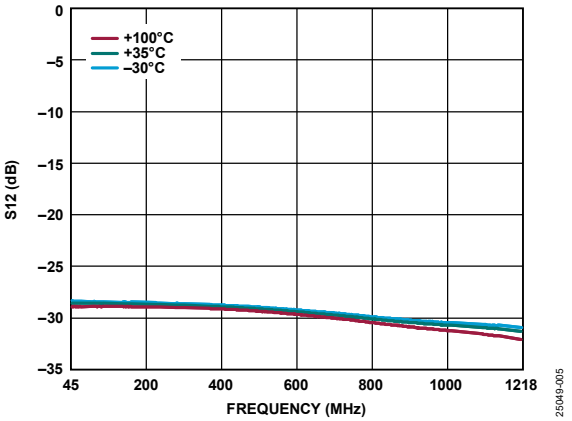

Figure 5. S12 vs. Frequency at Various Temperatures

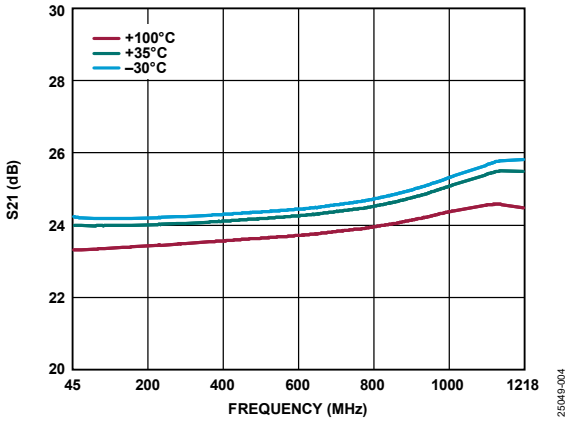

Figure 4. S21 vs. Frequency at Various Temperatures

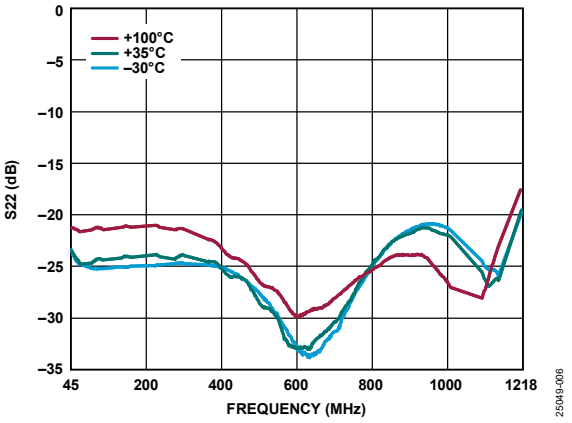

Figure 6. S22 vs. Frequency at Various Temperatures

18 dB TILT PERFORMANCE

18 dB extrapolated tilt and 190 digital channels (QAM256, ITU-T J.83, Annex B).

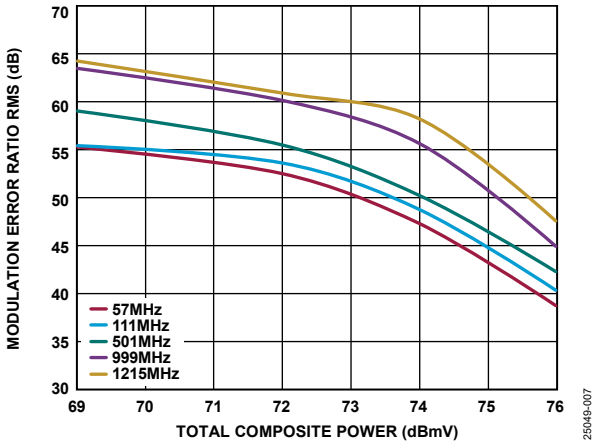

Figure 7. Modulation Error Ratio RMS vs. Total Composite Power at Various Frequencies, 35°C, 18 dB Tilt

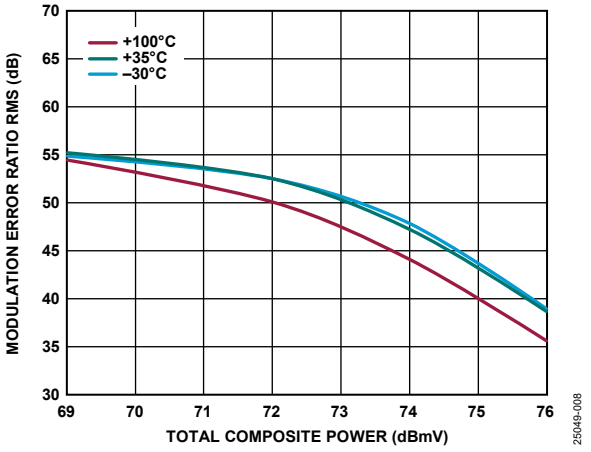

Figure 8. Modulation Error Ratio RMS vs. Total Composite Power at Various Temperatures, 57 MHz, 18 dB Tilt

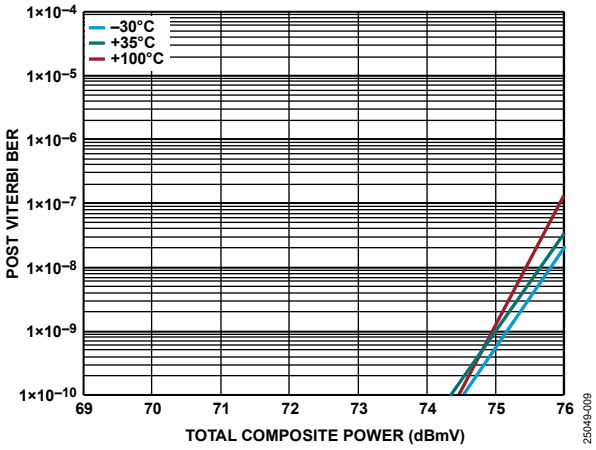

Figure 9. Post Viterbi BER vs. Total Composite Power at Various Temperatures, 57 MHz, 18 dB Tilt

THEORY OF OPERATION

The ADCA3950 is a 75 Ω input and output matched module designed for CATV applications. The ADCA3950 uses cascode field effect transistor (FET) feedback amplifiers in a Class A push pull configuration. The bottom half of the cascode stages are implemented in a single-die linear FET process that minimizes parasitics, thereby enabling higher gain. The top devices in the cascodes are implemented using a linear GaN process able to swing high RF voltages. The frequency of operation is from 45 MHz to 1218 MHz.

Internally, the ADCA3950 module uses a balun to convert the input signal to a balanced signal that feeds the active stages. An output impedance transformer and balun combination converts the balanced GaN signals to an unbalanced 75 Ω output. The output transformer also feeds the dc to the active stages and cancels second-order distortion products coming from the active devices.

The ADCA3950 is unconditionally stable and includes transient and surge protection circuits for robust operation in systems targeting DOCSIS 3.1 and legacy DOCSIS standards.

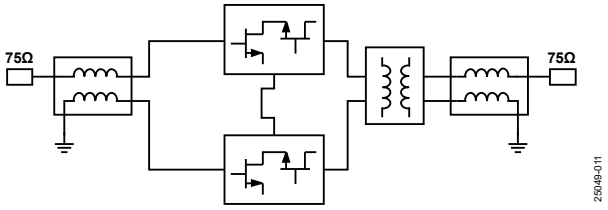

Figure 10. Simplified Schematic

APPLICATIONS INFORMATION

Basic connections for operating the ADCA3950 are shown in Figure 11. Both the INPUT pin (Pin 1) and the OUTPUT pin (Pin 9) of the ADCA3950 are matched to 75 Ω. The VCC pin (Pin 5) requires 24 V for typical operation.

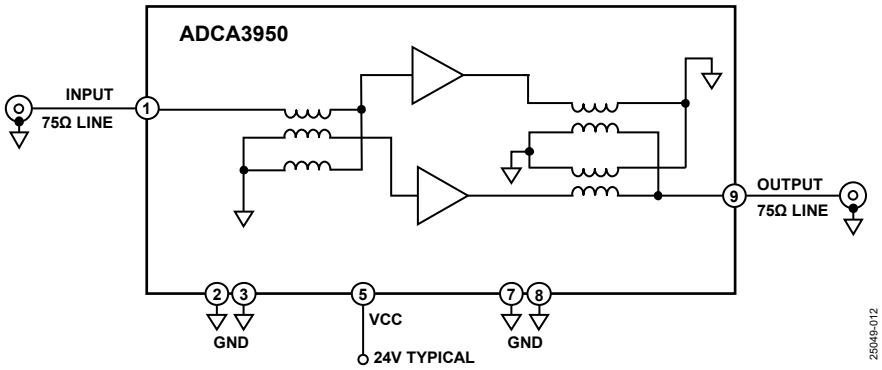

Figure 11. Basic Connections

OUTLINE DIMENSIONS

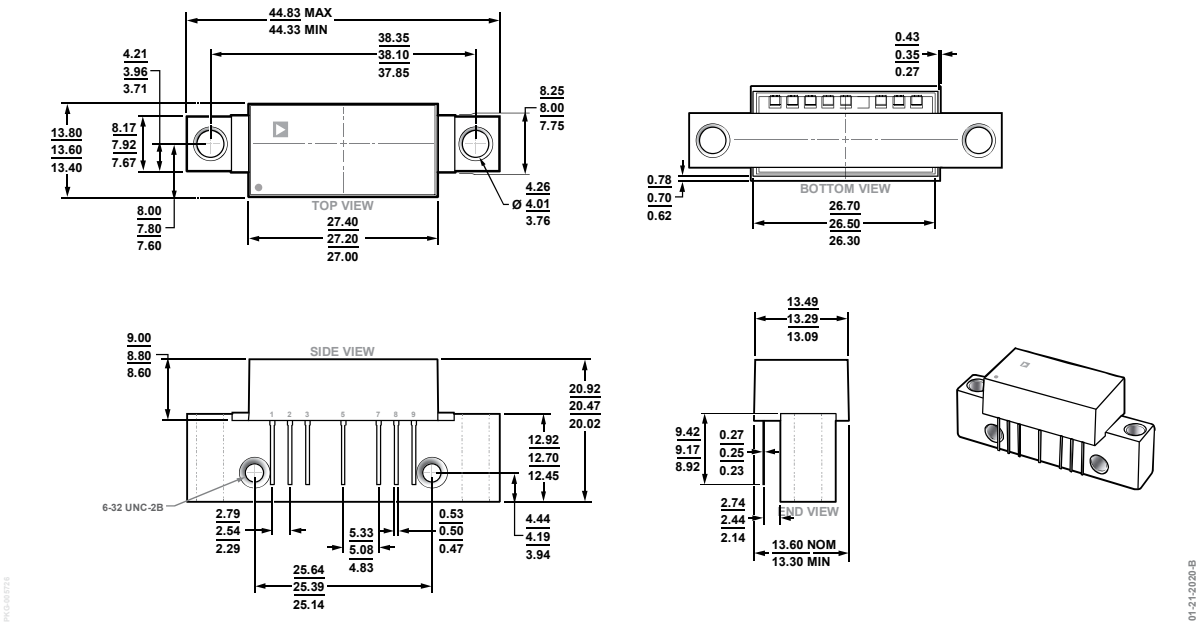

Figure 12. 7-Pin SOT-115J Module Package [MODULE]
(ML-7-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADCA3950AMLZ	−30°C to +100°C	7-Pin SOT-115J Module Package [MODULE], Box with 25 Pieces	ML-7-1

[1] Z = RoHS Compliant Part.

NOTES

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
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