

Ceramic Balance Filter

50Ω 4650 to 5150 MHz

BBFCV-492+



Generic photo used for illustration purposes only

CASE STYLE: JV1210C-4

+RoHS Compliant

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Available Tape and Reel at no extra cost

Reel Size	Devices/Reel
7"	20, 50, 100, 200, 500, 1000, 2000

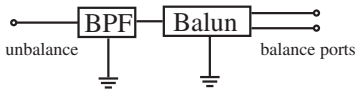
Features

- Small size (0.126"x0.098"x0.039")
- Temperature stable
- Hermetically sealed
- LTCC construction

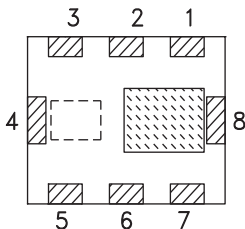
Applications

- 5G
- Cellular

Simplified Schematic



Top View



Pad Connections

Unbalanced Port	7
Balanced Port	3, 5
GND	2, 4, 8
GND or DC Feed	6
NC	1

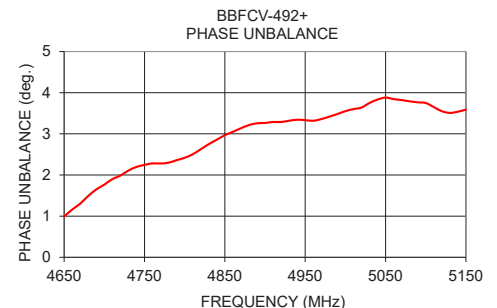
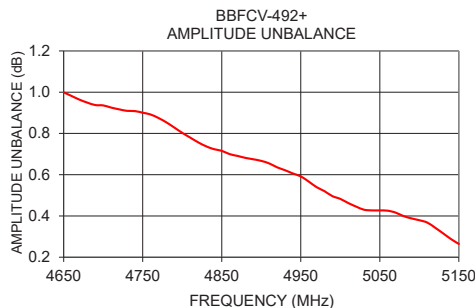
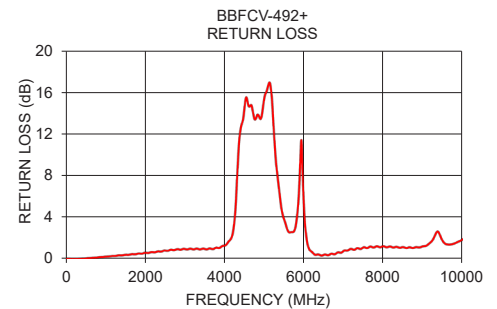
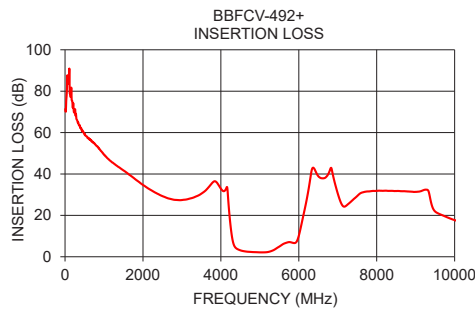
Electrical Specifications at 25°C

Parameter	Frequency (MHz)	Min.	Typ.	Max.	Unit
Impedance Ratio			2:1		
Insertion Loss	4650 - 5150	—	—	3.5	dB
Attenuation	50-1098	28	—	—	dB
	1098-4000	20	—	—	
	6696-8049	22	—	—	
	9645-12750	10	—	—	
Amplitude Unbalance	4650-5150	—	—	1.3	dB
Phase Unbalance	4650-5150	—	—	12	degree
Input VSWR	4650-5150	—	1.67	—	

Maximum Ratings

Operating Temperature	-55°C to +105°C
Storage Temperature ¹	-55°C to +105°C
RF Power Input ²	1W @25°C

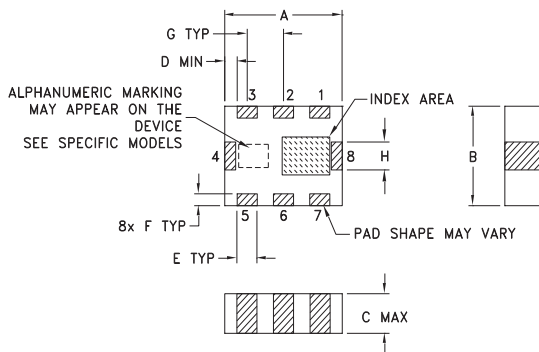
1. Refer to product storage temperature after installation
Suggestion for T&R unused product storage condition: +5 ~ +35 °C, Humidity 45~75%RH, 12 month Max
2. Derate linearly to 0.5W at 85°C



Typical Performance Data

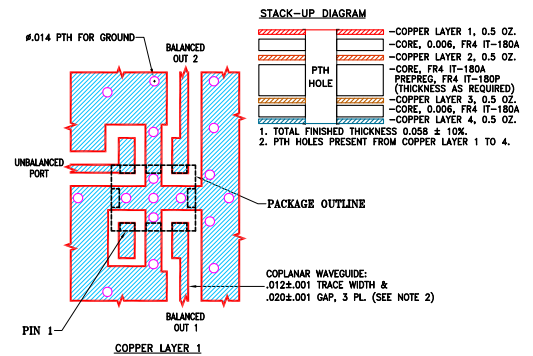
Frequency (MHz)	Insertion Loss (dB)	Return Loss (dB)	Amplitude Unbalance (dB)	Phase Unbalance (Deg.)
10	71.41	0.06	1.38	100.60
50	81.78	0.04	2.23	151.82
100	83.48	0.04	8.13	134.82
500	59.00	0.08	9.62	168.96
1000	49.41	0.26	10.86	120.62
2000	34.69	0.62	1.97	57.65
3000	27.42	1.00	3.11	6.88
3500	30.50	1.00	1.03	40.22
4000	32.88	1.31	3.27	90.58
4650	2.52	14.66	1.00	1.33
5150	2.17	16.82	0.26	3.55
6000	10.14	5.42	0.91	0.65
7000	30.56	0.79	4.17	74.13
8000	31.83	1.25	1.36	63.10
9000	31.36	1.24	4.95	80.75
10000	17.71	1.88	3.06	167.42

Outline Drawing



Suggested Layout, Tolerance to be within .002

Demo Board MCL P/N: TB-1053+ Suggested PCB Layout (PL-632)



- NOTES:
- PCB IS MULTILAYER PCB, SEE STACK-UP DIAGRAM.
 - TRACE WIDTH & GAP PARAMETERS ARE SHOWN FOR FR4 IT-180A WITH DIELECTRIC THICKNESS .006"±.0007"; COPPER: 1/2 OZ. FOR OTHER MATERIALS TRACE WIDTH AND GAP MAY NEED TO BE MODIFIED.
 - LAYERS 2,3,4 OF THE PCB ARE CONTINUOUS GROUND PLANE.

■ DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK

Outline Dimensions (inch/mm)

A	B	C	D	E	F	G
.126	.098	.039	.004	.022	.012	.039
3.2	2.5	1.0	0.1	0.56	0.3	1.0
H	J	K	L	M	wt	
.028	.031	.024	.130	0.15	grams	
0.7	0.8	0.6	3.30	3.81	0.030	

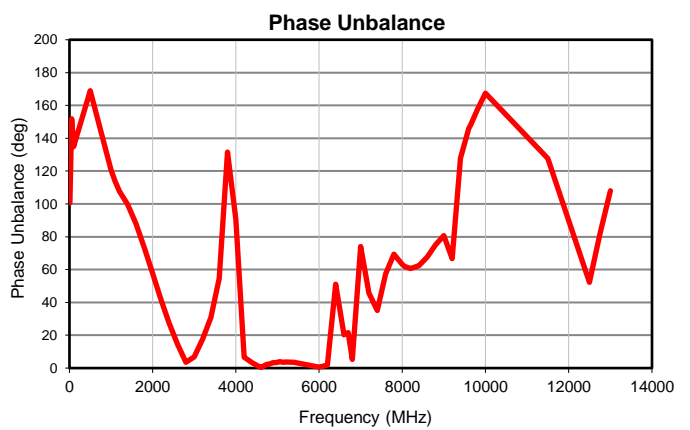
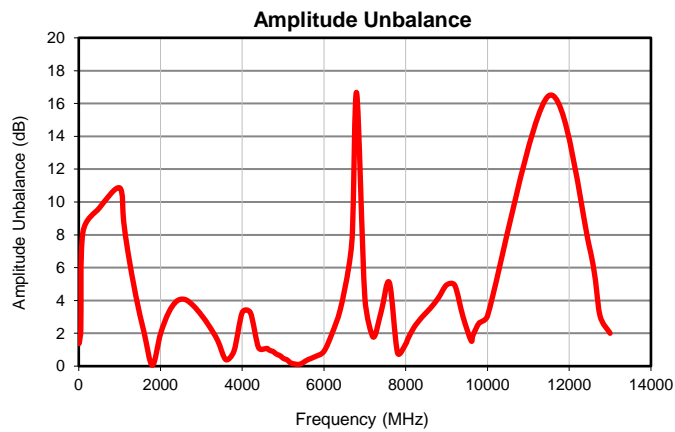
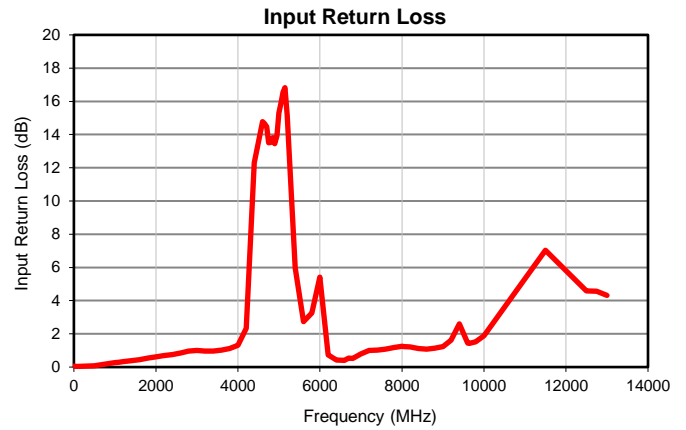
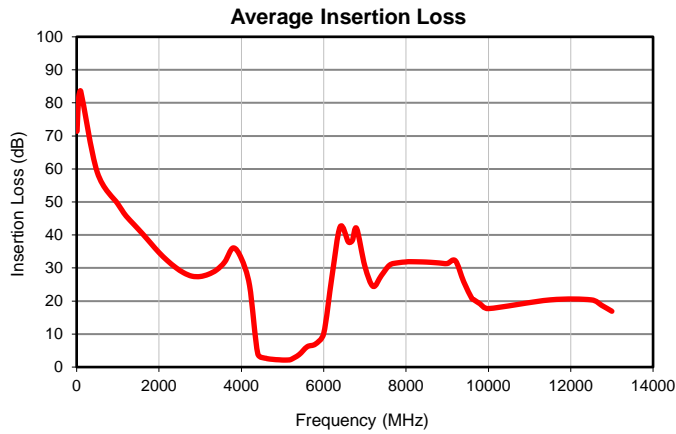
Additional Notes

- Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
- Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
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Typical Performance Data

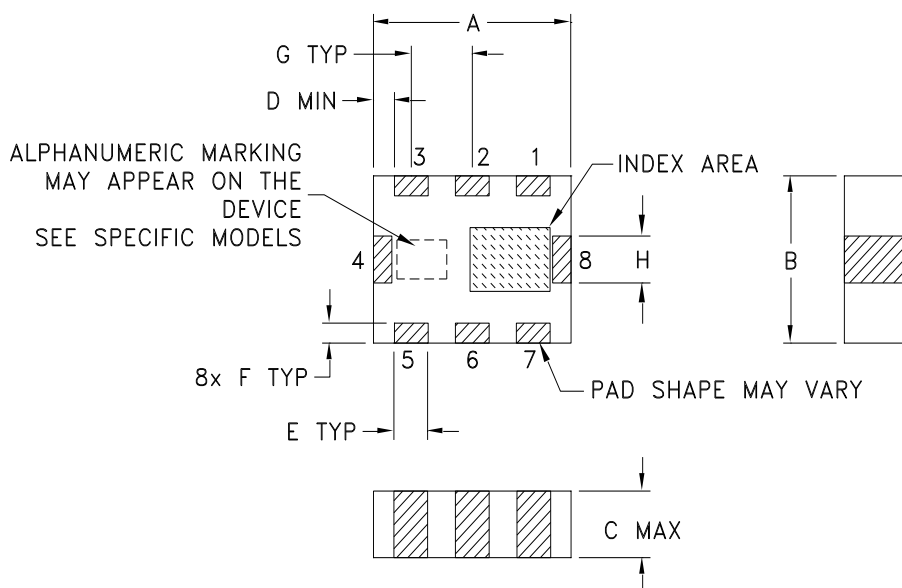
FREQUENCY (MHz)	INSERTION LOSS (dB)	RETURN LOSS (dB)	AMPLITUDE UNBALANCE (dB)	PHASE UNBALANCE (deg.)
10	71.41	0.06	1.38	100.60
50	81.78	0.04	2.23	151.82
100	83.48	0.04	8.13	134.82
500	59.00	0.08	9.62	168.96
1000	49.41	0.26	10.86	120.62
1098	47.57	0.28	8.82	113.65
1200	45.75	0.32	7.01	107.89
1400	43.06	0.38	4.24	99.57
1600	40.37	0.45	2.03	87.87
1800	37.51	0.53	0.05	73.31
2000	34.69	0.62	1.97	57.65
2200	32.27	0.68	3.27	41.80
2400	30.20	0.75	3.97	27.15
2600	28.55	0.85	4.06	14.47
2800	27.53	0.96	3.69	3.42
3000	27.42	1.00	3.11	6.88
3200	28.10	0.96	2.41	17.58
3400	29.43	0.96	1.56	30.75
3600	31.88	1.02	0.39	54.50
3800	36.08	1.11	0.93	131.67
4000	32.88	1.31	3.27	90.58
4200	24.67	2.34	3.26	6.62
4400	4.00	12.29	1.12	3.12
4600	2.66	14.78	1.08	0.36
4650	2.52	14.66	1.00	0.99
4700	2.41	14.47	0.94	1.76
4750	2.36	13.50	0.90	2.25
4800	2.29	13.52	0.80	2.42
4850	2.24	13.82	0.72	2.97
4900	2.21	13.45	0.67	3.26
4950	2.17	13.93	0.59	3.33
5000	2.13	15.29	0.48	3.55
5050	2.12	15.94	0.43	3.88
5100	2.13	16.55	0.38	3.75
5150	2.17	16.82	0.26	3.59
5200	2.27	15.16	0.18	3.72
5400	3.73	5.97	0.11	3.46
5600	6.16	2.73	0.38	2.49
5800	6.98	3.25	0.60	1.53
6000	10.14	5.42	0.91	0.65
6200	27.35	0.73	2.01	1.81
6400	42.46	0.43	3.46	51.14
6600	37.90	0.40	5.95	20.34
6696	38.33	0.53	8.15	21.56
6800	41.96	0.52	16.63	5.21
7000	30.56	0.79	4.17	74.13
7200	24.44	1.00	1.77	45.67
7400	27.70	1.02	3.33	35.10
7600	30.86	1.08	5.08	57.33
7800	31.58	1.18	0.81	69.34
8000	31.83	1.25	1.36	63.10
8049	31.91	1.23	1.64	62.06
8200	31.89	1.21	2.35	60.63
8400	31.84	1.12	2.99	62.43
8600	31.72	1.08	3.52	67.71
8800	31.53	1.13	4.16	75.08
9000	31.36	1.24	4.95	80.75
9200	32.18	1.62	4.92	66.64
9400	25.88	2.60	3.03	127.91
9600	20.74	1.44	1.55	145.93
9645	20.42	1.42	1.88	148.08
9800	19.13	1.52	2.64	157.05
10000	17.71	1.88	3.06	167.42
11500	20.35	7.03	16.47	127.77
12500	20.35	4.58	7.20	52.15
12750	18.71	4.57	3.11	81.86
13000	16.90	4.32	2.00	108.00

Typical Performance Data

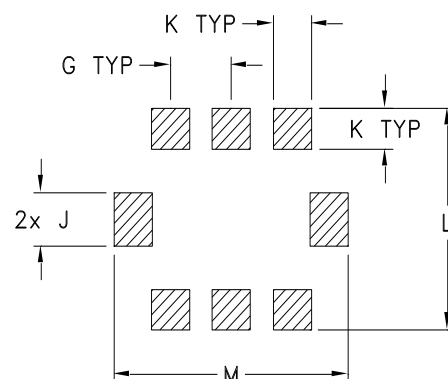


Outline Dimensions

JV1210C-4



PCB Land Pattern



Suggested Layout,
Tolerance to be within $\pm .002$

CASE #	A	B	C	D	E	F	G	H	J	K	L	M	WT. GRAM
JV1210C-4	.126 (3.2)	.098 (2.5)	.039 (1.00)	.004 (.1)	.022 (.56)	.012 (.3)	.039 (1.0)	.028 (.71)	.031 (.79)	.024 (.61)	.130 (3.30)	.150 (3.81)	.03

Dimensions are in inches (mm). Tolerances: 2 Pl. $\pm .01$; 3 Pl. $\pm .005$

Notes:

- Open style, ceramic base.
- Termination finish: **as shown below or indicated on Data Sheet.**
For RoHS Case Styles: Matte-Tin. All models, (+) suffix.
For RoHS-5 Case Styles: Tin-Lead plate. All models, no (+) suffix.
- Pad tolerance is non-cumulative. Minimum spacing between each pad is .004.



P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 For detailed performance specs & shopping online see Mini-Circuits web site



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RF/IF MICROWAVE COMPONENTS

Tape & Reel Packaging TR-F74

DEVICE ORIENTATION IN T&R

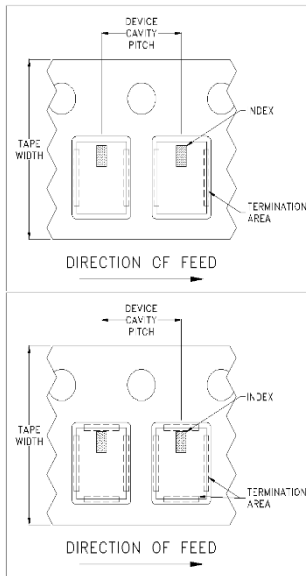


ILLUSTRATION 1

Applicable Case Styles

GE0805C-1
GE0805C-1AP
JV1210C-1
GU2939

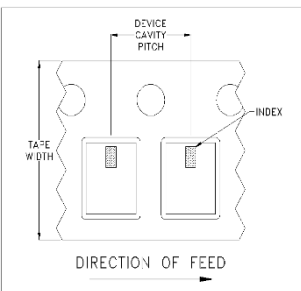


ILLUSTRATION 2

Applicable Case Styles

JV1210C
JV1210C-2
JV1210C-3
JV1210C-4
JV1210C-5
JV1210C-6
JV1210C-11

ILLUSTRATION 3

Applicable Case Styles

JC0603C-8
JC0603C-9
JV1210C-7
JV1210C-8
JV1210C-9
JV1210C-10
JV1210C-13
GE0805C-13
GE0805C-19
GE0805C-20

Tape Width, mm	Device Cavity Pitch, mm	Real Size, inches	Devices per Reel	
8	4	7	Small quantity standards (see note)	20
				50
				100
				200
				500
				1000
			Standard	2000
				4000

Note: Small reel availability varies by model. Refer to pricing and availability on individual model dashboard.

Mini-Circuits carrier tape materials provide protection from ESD (Electro-Static Discharge) during handling and transportation. Tapes are static dissipative and comply with industry standards EIA-481/EIA-541.

Go to: www.minicircuits.com/pages/pdfs/tape.pdf



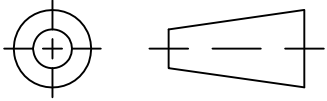
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THIRD ANGLE PROJECTION

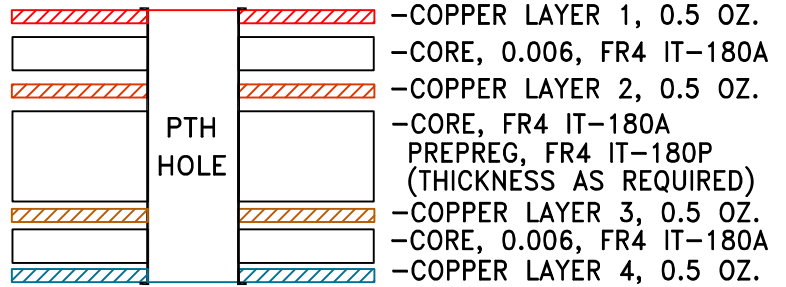


REVISIONS

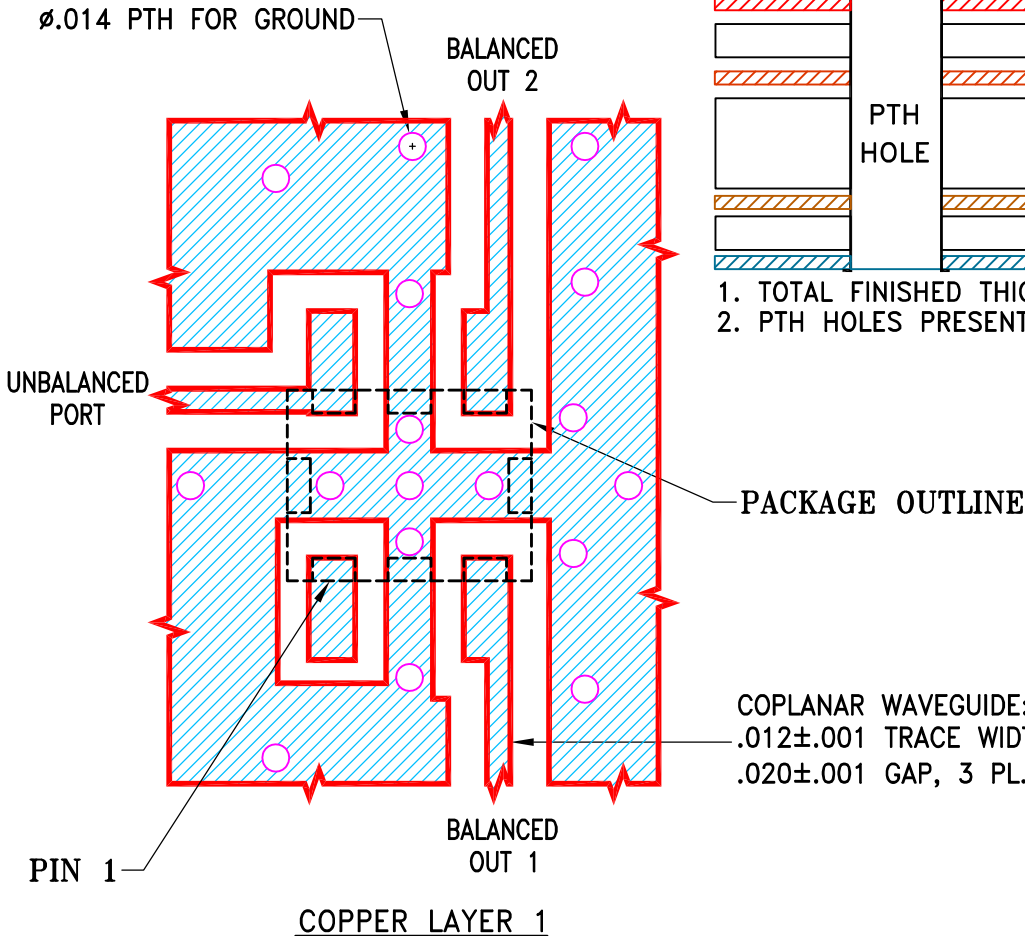
REV	ECN No.	DESCRIPTION	DATE	DR	AUTH
OR	M174716	NEW RELEASE	06/10/19	ITG	SL

SUGGESTED MOUNTING CONFIGURATION FOR JV1210C-4 CASE STYLE

STACK-UP DIAGRAM

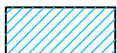


- TOTAL FINISHED THICKNESS 0.058 ± 10%.
- PTH HOLES PRESENT FROM COPPER LAYER 1 TO 4.



NOTES:

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- TRACE WIDTH & GAP PARAMETERS ARE SHOWN FOR FR4 IT-180A WITH DIELECTRIC THICKNESS .006"±.0007"; COPPER: 1/2 OZ. FOR OTHER MATERIALS TRACE WIDTH AND GAP MAY NEED TO BE MODIFIED.
- LAYERS 2,3,4 OF THE PCB ARE CONTINUOUS GROUND PLANE.



DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK

UNLESS OTHERWISE SPECIFIED	INITIALS	DATE
DIMENSIONS ARE IN INCHES TOLERANCES ON: 2 PL DECIMALS ± 3 PL DECIMALS ± .005 ANGLES ± FRACTIONS ±	DRAWN	ITG 06/04/19
	CHECKED	GF 06/10/19
	APPROVED	SL 06/10/19



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PL, JV1210C-4, TB-BLFCV/BBFCV

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SIZE	CODE IDENT	DRAWING NO:	REV:
A	15542	98-PL-632	OR
FILE:	98PL632	SCALE: 10:1	SHEET: 1 OF 1

All Mini-Circuits products are manufactured under exacting quality assurance and control standards, and are capable of meeting published specifications after being subjected to any or all of the following physical and environmental test.

Specification	Test/Inspection Condition	Reference/Spec
Operating Temperature	-55° to 105°C Ambient Environment	Individual Model Data Sheet
Storage Temperature	-55° to 105°C Ambient Environment	Individual Model Data Sheet
Humidity	90 to 95% RH, 240 hours, 50°C	MIL-STD-202, Method 103, Condition A, Except 50°C and end-point electrical test done within 12 hours
Solder Reflow Heat	Sn-Pb Eutectic Process 225°C peak Pb-Free Process 245° - 250°C peak	J-STD-020C, Table 4-1, 4-2 and 5-2, Figure 5-1
Solderability	10X Magnification	J-STD-002, Para 4.2.5, Test S, 95% Coverage
Vibration (High Frequency)	20g peak, 10-2000 Hz, 12 times in each of three perpendicular directions (total 36)	MIL-STD-202, Method 204, Condition D
Mechanical Shock	50g, 11 ms, 1/2-sine, 18 shocks: 3 each direction, each of 3 axes	MIL-STD-202, Method 213, Condition A