# A Practical Approach to the Design and Implementation of Scalable, High-Performance, Custom SMT Packages for mmWave Applications

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Abstract—After many years of research and development, electrical engineers, physicists, mathematicians and scientists have come to realize the benefits of operating communications systems at higher frequencies. Some of the most notable advances stemming from this research include: smaller circuit implementations for the same functionality; improved antenna gain for a given antenna size; and dramatic increases in data-carrying capacity. However, numerous challenges remain in implementing high-frequency circuits under real-world constraints. Among the non-trivial problems, packaging stands out.

It is critical that packages for RF components allow the integration of multiple circuital technologies while achieving the best possible balance of performance and cost for a given application. Nevertheless, traditional packaging techniques have proven incapable of translating the same performance typically seen below X-band into the millimeter wave range due to embedded parasitics and other inherent technological constraints. These limitations have led the design community to leverage new packaging technologies, novel design methodologies, and advanced CAD tools to develop cost-effective, scalable packaging solutions for high-frequency markets and applications. These new packaging techniques are now moving away from performancedegrading implementations such as molding compounds and long wire bonding structures to achieve outstanding performance beyond 55 GHz. In light of these developments, this paper explores some of the key concepts underlying the development of commercially viable packaging solutions for millimeter wave components (patent pending).

*Index Terms*—Low-Temperature Co-Fired Ceramic, LTCC MMIC, mmWave, Multi-Physics, Simulation, SMT Package, Packaging

#### I. INTRODUCTION

Global mobile data usage is expected to grow from 11.2 Petabytes/month in 2017 to 48.3 Petabytes/month in 2021. 5G has emerged as a strong proposal to achieve a  $1000 \times$  increase in mobile data capacity and support the expected data consumption of seven billion people and seven trillion devices while remaining energy efficient and maintaining nearly-zero downtime[1]. The advent of 5G has brought about increasing development of integrated circuits (ICs) to meet the requirements for high frequency applications and a related need to develop cost-effective packages that not only protect the ICs, but are also capable of maintaining good electrical performance across wide operational frequency bands.

Current surface mount QFN packages are not suitable for packaging devices at millimeter wave frequencies. Parasitic



Fig. 1. Schematical cross section of ceramic package.

elements encountered in the signal path, for example discontinuities in the vertical transition from the PCB to the top side of the QFN and the wire bond to the IC, are negligible at lower frequencies but become relevant once the physical dimensions of the elements become a fraction of the wavelength. Another drawback of QFN packages is their reliance on over-molding, which not only increases electrical loss at higher frequencies, but also makes it impossible to package die featuring air-bridges. Moreover, QFN packages are incapable of accommodating flip chip devices due to their standardized nature. Many solutions have been developed in order to address these challenges: Air cavity QFN packages allow for ICs with air-bridges, but still lack a well-matched transition at high frequencies. MicroCoax structures [2] allow for high frequency operation, but require specialized assembly processes. Custom packaging solutions can compensate for parasitic effects [3] and allow for air-cavity implementation. Fully-custom solutions are most viable when incorporated into a rapid, low-risk design strategy as well as a highly-automated assembly process.

Modern RF applications have stringent requirements for components beyond electrical specifications; dense assemblies, high operating powers, and the need for robust, reliable systems place heavy demands on MMIC package designers to balance electrical performance with desirable thermal and mechanical characteristics. Since design features which benefit one aspect of performance may detract from the requirements of others, tradeoffs are often necessary. For example, a tradeoff intended to improve electrical performance at the expense of heat dissipation may yield little benefit due to the effect of



Fig. 2. Schematical cross section of organic package.



Fig. 3. Lumped element representation of the gold wire interconnect between the package pad ( $C_{\rm PK}$ ), the gold wire ( $L_{\rm WB}$ ) and the IC pad ( $C_{\rm IC}$ )

a temperature rise on conductors and semiconductors. It is therefore critical for designers to understand the simultaneous effects of design choices on the different aspects of a device's performance.

In this paper, we present the development of custom surfacemount packages with good electrical performance from DC to 50 GHz, accounting for the PCB, the surface mount package, and the IC (patent pending). Section II describes the package's components and design. Section III discusses the trade-off between customization and standardization of design features in the context of performance and cost goals. Measured performance of a broadband MMIC attenuator die in both custom organic and LTCC packages are shown. Additionally, the benefits of a multi-physics simulation workflow employed in the design of these packages are discussed.

# II. DESIGN

#### A. Structure

Schematical cross section diagrams of the ceramic and organic packages and PCB are shown in Fig. 1 and Fig. 2, respectively. The following description is common to both. The IC is attached to the pocket inside the substrate using conductive epoxy. This implementation minimizes the length of the gold wirebonds. The gold wire interconnects the RF pads of the IC and the RF pads of the package, forming the low-pass network depicted in Fig. 3, where the wirebond is represented as a lumped series inductance  $L_{\rm WB}$ , and the pads are represented as  $C_{\rm PK}$  and  $C_{\rm IC}$ . Proper tuning of this matching network is critical for an accurate impedance match and good wideband electrical performance. The package's RF pad is followed by a microstrip line with 50  $\Omega$  characteristic impedance, and a matched vertical transition down to the bottom pad. The bottom pad of the package is made to

have a 50  $\Omega$  characteristic impedance in a Grounded Coplanar Waveguide (CPWG) configuration. The package is soldered to the PCB, which has GCPW with a 50  $\Omega$  characteristic impedance. A plastic or ceramic lid is attached to the package with a non-conductive B-staged epoxy.

# B. Materials

Material and technology selection play a big role in the performance of a package. The selection of the right materials will depend on the application requirements such as hermeticity, maximum operating frequency, package size, package weight, first- and second-level interconnects, thermal management constraints, and tolerable insertion loss of interconnects [4].

In both the LTCC and organic substrate packages, the selection of substrate material must take into account the dielectric constant and loss tangent needed to achieve the desired RF performance. The substrate also determines the package topology and the compatibility with the other materials. The two substrates explored here are LTCC and organic substrate. The LTCC package, Fig. 1, consists of a ceramic monolithic structure with a cavity formed in the top tape layers of the substrate. The exposed top face of the pocket features a continuous metallization that is connected to the bottom ground pad through multiple vias. Being a stiffer material, it is easier to wire bond. In the case of the organic package, Fig. 2, the pocket is created by removing a portion of the substrate and exposing the bottom metallization, allowing for better RF grounding and thermal resistance.

In both packages, the conductor materials and finishes are selected to achieve good RF performance and to accommodate industry-standard assembly processes. The metal conductor on the LTCC package is typically silver with an Electroless Nickel Immersion Gold (ENIG) surface finish. The plating protects the underlying silver from oxidation and must also have properties compatible with soldering and wirebonding processes. The organic package employs copper conductors and may feature any of several different surface finishes. The choice of surface finish may be a critical matter in high frequency applications, as both surface roughness and electrical conductivity have significant effects on insertion losses [5] [6].

The selection of the conductive epoxy used to mount the MMIC die has a significant impact on the total thermal resistance of the package. As the main point of contact between the die and the package, the epoxy facilitates the majority of the die's heat dissipation.

#### C. Simulation Workflow

During the design phase of this project, the electrical, thermal, and mechanical performance of the LTCC and organic packages were analyzed using a multi-physics simulation workflow. The simulation workflow employed multiple simulators which were operated sequentially, with each simulator's results being used as part of the next simulator's setup.

The specific simulation workflow is as follows:



Fig. 4. Electromagnetic simulation model of LTCC package, including only the design elements relevant to electrical performance.



Fig. 5. Close-up of geometry and mesh employed in thermal and mechanical simulations of LTCC package, with package lid hidden. Note that the model includes solder, die-attach epoxy, and both hollow and solder-filled PTHs.

- 1) A full 3D finite-element electromagnetic simulation is performed on a simplified version of the design's geometry. The simulation yields S-parameter data and a spatial distribution of power dissipation within the design.
- 2) A full 3D finite-element thermal simulation is run on the electromagnetic simulation's model, augmented to include geometry relevant to thermal and mechanical (but not electrical) performance. As shown in Fig. 5, effort was made to accurately model critical regions of simulation geometry, such as hollow and solder-filled PTHs. The simulation employs the power dissipation computed from the electromagnetic simulation and yields a temperature distribution within the model's geometry.
- 3) A full 3D finite-element mechanical simulation is run on the full model geometry, employing the spatial temperature distribution as part of its setup. The simulation yields mechanical strains and stresses within the model geometry.
- 4) If desired, the above process may be iterated until convergence criteria are met, feeding the temperature rise information and model geometry deformation into the electrical simulator for the next pass. In practice, a single pass is often sufficient to achieve outstanding agreement between simulation results and physical measurements.

While more complex than a workflow involving separate electrical, thermal, and mechanical simulation tasks, a true

multi-physics simulation workflow provides design engineers with a holistic view of a design's performance. For example, a traditional thermal simulation of a microstrip conductor may involve a uniformly-distributed heat source applied to the conductor's volume or faces. Such an approach discards valuable information about localized heat generation, since current densities at millimeter-wave frequencies are nonuniform. A multi-physics simulation approach implicitly captures this effect and others without needing attention from the designer.

The ability of a multi-physics simulation to automatically account for conditions too complex to set up manually is especially valuable for LTCC designs. As LTCC designs consist of a monolithic ceramic structure with complex internal conductor geometry, thermal images of the exterior of such a device may not fully reveal its internal thermal behavior.

Because the electrical, thermal, and mechanical aspects of a design's performance are often linked (due to temperaturedependent electrical resistivities, thermal expansion, and so on), such a simulation workflow makes it possible to best understand the impact of design decisions on interrelated aspects of performance. The workflow has been qualified through multiple projects involving several technologies, and achieves simulation results in very close agreement with performance measurements. As with other portions of Mini-Circuits' established LTCC process, it is subject to continual evaluation and improvement.

# III. CUSTOMIZATION VS. STANDARDIZATION

Although the QFN package has been an industry workhorse for both active and passive electronic components up to V-band [7], its highly-standardized nature makes it a suboptimal solution for some applications. As applications march towards millimeter-wave frequencies, packaging technologies must adapt to widely-varying industry needs.

While a one-size-fits-all solution may fit all applications equally poorly, a fully-custom solution yielding outstanding results may be cost- and time-prohibitive. To develop a rapid, cost-effective packaging solution which still offers outstanding application flexibility, it was desirable to combine industrystandard processes and tunable design features into a customizable package template. This 'templated' approach to package design allows for the reuse of proven design elements, reducing the effort and risk incurred by from-scratch solutions. Facilities for adaptation to an application's specific electrical, thermal, mechanical, and environmental needs are provided while minimizing or eliminating the need for extensive qualification of new designs.

QFN packages are typically available in a granular range of standardized sizes  $(3 \text{ mm} \times 3 \text{ mm}, 4 \text{ mm} \times 4 \text{ mm}, \text{ and so}$ on), while a MMIC die may be any size and aspect ratio. A die that is slightly too large to fit one standard QFN package size must instead use the next size up, necessitating long wirebonds with correspondingly large parasitic inductances. The package itself offers little facility to compensate for these parasitics, a task relegated instead to conductor geometry on the PCB and die. Furthermore, QFN packages employ a plastic encapsulant which envelops the leadframe, die, and wirebonds. Delicate structures on the MMIC die such as air bridges are incompatible with such an encapsulation process; even in the absence of incompatible MMIC features, the encapsulant may detune or degrade the performance of sensitive electronics simply by proximity. Finally, the terminals of the QFN package are highly standardized with little flexibility of the pad sizes and geometries. For some applications, the electrical parasitics associated with the fixed transition geometry may be unacceptable.

Mini-Circuits' custom LTCC and organic substrate packages address the above limitations, offering solutions with sufficient flexibility to meet the needs of a wide variety of applications. In these packages, the die inhabits a pocket atop the substrate as shown in Fig. 1 and Fig. 2. The pocket's dimensions are specified according to the customer's die so that wirebond pads can be brought as close to the die as possible, minimizing bondwire length and inductance. Therefore the LTCC and organic substrate packages offer greater flexibility with regard to MMIC die sizes even though they are currently available in the same sizes as standard QFN packages,  $3 \text{ mm} \times 3 \text{ mm}$ ,  $4 \text{ mm} \times 4 \text{ mm}$ , and  $5 \text{ mm} \times 5 \text{ mm}$ . A plastic lid is affixed over the die and wire bonds with a B-staged epoxy compound, maintaining an air gap above the die and wirebonds and achieving a semi-hermetic seal. The use of an air gap rather than an encapsulant permits the packaging of delicate MMIC structures and minimizes degradation of electrical performance.

Unlike QFN packages, the LTCC and organic substrate packages offer the flexibility needed to best suit a wide variety of applications. The package structure contains tunable elements which electrically compensate for the parasitics associated with the transitions from the PCB to the package and from the package to the MMIC die. Furthermore, since the package features printed conductors rather than a solid leadframe, the footprints of the LTCC and organic substrate packages can be customized with minimal tooling cost.

### IV. EXAMPLES

To validate the design and to measure the performance of the organic and LTCC packages, multiple packages were designed, fabricated, and tested. The packages were assembled and soldered on 5 mil Taconic TLY-5 evaluation PCBs with 50  $\Omega$  CPWG traces. 2.4 mm Southwest Microwave edgelaunch connectors were used to interface the PCBs with the Vector Network Analyser (VNA). Standard Short-Open-Load-Thru (SOLT) calibration was performed up to 55 GHz, up to the reference plane of the connectors. The insertion loss measurements for each package are normalized by subtracting the losses of the PCB thru-line.

#### A. MMIC 2 dB Attenuator on Organic Package

A 2 dB MMIC attenuator is mounted and wirebonded on top of an organic package. Fig. 6 shows the package mounted on top of the PCB, as well as a close up of the package without



Fig. 6. IC in organic package on evaluation board. (a) Package with lid on evaluation board. (b) Close-up of package without lid, showing flip chip die atop package substrate.



Fig. 7. Measurement results of 2 dB attenuator on organic package.

the lid, showing the die and the wirebonds. Fig. 7 shows the measured data of the device. The  $S_{21}$  trace shows a very flat response of -2 dB up to 48 GHz. A good return loss is also observed for the entire frequency bandwidth.

#### B. MMIC 2 dB Attenuator on Ceramic Package

A 2 dB MMIC attenuator is mounted and wirebonded on top of a ceramic package. Fig. 8 shows the package mounted on top of the PCB, as well as a close up of the package without the lid, showing the die and the wirebonds. Fig. 9 shows the measured data of the device. The  $S_{21}$  trace shows a very flat response of -2 dB up to 55 GHz. A good return loss is also observed for the entire frequency bandwidth.

### C. Flip-Chip SPDT Switch on Ceramic Package

A flip-chip SPDT switch is mounted on top of an organic package. Fig. 10 shows the package mounted on top of the PCB, as well as a close up of the package with the exposed flip-chip die. Fig. 11 shows the measured data of the device with the RF2 channel active. A good return loss is observed over the entire bandwidth.

#### V. CONCLUSION

Packages employing both LTCC and organic substrate materials have been developed (patent pending). Outstanding electrical performance of both packaging technologies has been



Fig. 8. IC in LTCC package on evaluation board. (a) Package without lid on evaluation board. (b) Close-up of package without lid, showing die and wirebonds.



Fig. 9. Measurement results of 2 dB attenuator on LTCC package.



Fig. 10. Packaged IC on evaluation board. (a) Package with lid on evaluation board. (b) Close-up of package without lid, showing die and wirebonds.

demonstrated up to 55 GHz. Both packaging methodologies accommodate a wide variety of application-specific needs, including impedance-matching, variable die sizes, and a wide range of IO pad counts, signal types (DC or RF), and PCB geometries. By combining standardized and adjustable features into a tunable package template, Mini-Circuits' approach to packaging achieves desirable electrical performance and broad applicability while minimizing turnaround time, cost, and risk.

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Fig. 11. Measurement results SPDT flip-chip switch with RF2 channel active.

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