Mini-Circuits®

ISC-2425-25+ Coherence Application Note

AN-50-004

www.minicircuits.com

Introduction

This document describes the steps to setup coherent operating mode amongst an arbitrary number of Mini-Circuits ISC-2425-25+ signal generators.
To achieve coherence, a cable to connect the modules and share the clock signal and software configuration steps is necessary. See **Figure 1**.

Note that when the different ISC boards lock in coherent mode their respective starting phase difference with respect to each other is unknown. The user should then adapt the phase on each slave channel for the intended process target e.g., minimum total sum of reflected powers.
This phase relation will change every time the boards move out of- and return back to coherent mode.

NOTE: The phase relation will not change while in coherent mode. A reset of the board will also cause a new lock condition.

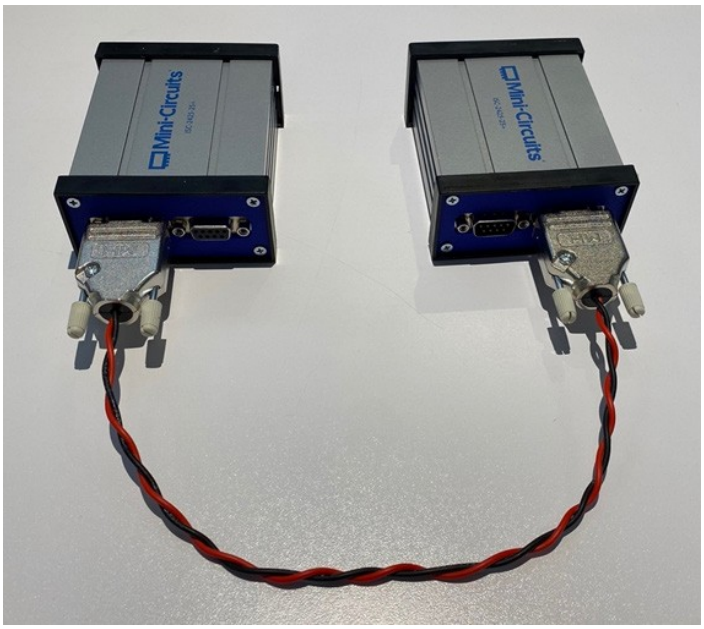

Figure 1: Two ISC-2425-25+'s connected in Coherent Mode

Hardware requirements

To achieve coherence amongst several RF generators, the all the ISCs need to run off the same time base. This is achieved by daisy chaining a low frequency (10 MHz) clock via a differential MLVDS bus. One of the ISC boards will be the master, the others will be slaves.

A CABLE CONNECTS THE BUS AMONGST THE UNITS:

A cable with a DE-9 (9-pin D-sub) male and female connector at either end needs to be produced. Pins 1 and 6 need to be connected straight through (see images). A ground connection is provided via the controlling computer (USB cables) or alternatively by also connecting pin3 in the DE-9 connectors. See **Figure 2**.

The master channel connects through the male DE-9 (on the board) to the female DE-9 on the slave board. The master ISC typically sits at either end of the chain of ISC units that need to work coherently. However, it is possible to completely close the clock distribution chain to have any ISC in the chain to become the master and the others slaves, consequently.

There can be several masters in each clock distribution chain as well – all the units downstream of the masters will be coherent slaves with respect to the upstream master. The clock link from a “last” slave into a next master will have no effect.

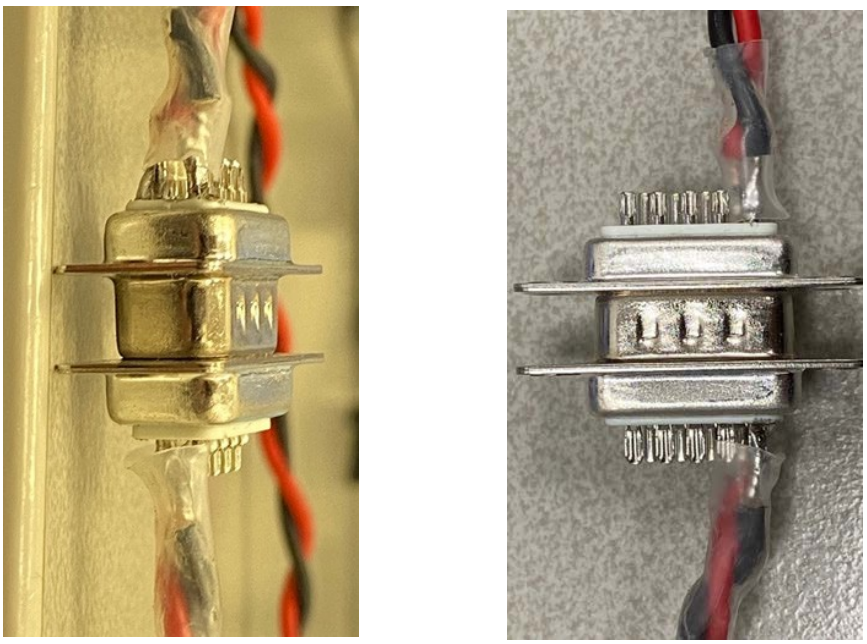

Figure 2: Male- and female subD 9 connectors and wiring(pin 1,6, and optionally 3) straight through.

Software Setup

1. After daisy chaining two or more ISC boards together using the set of male & female DE-9 connectors on the rear of the boards (see **Figure 2** above). They are ready to be setup for coherent mode operation.

2. Now the clock source setting of all ISC boards must be configured.

- The first board in the chain must be configured as a master. All the remaining boards shouldbe configured as inline slaves.
- To configure the clock source setting of the ISC boards, please see the following commanddescription.

$CSS – SET CLOCK SOURCE

This command sets the clock source configuration of the ISC board into either stand alone, master,slave or inline-slave mode.

SYNTAX:

Input:	$CSS, [channel] , [clock source]
Output:	$CSS, channel], OK

- **[channel]** – Channel identification number.
- **[clock source]** – Numeric value assigned clock source configuration.

0 – Standalone (default):
Use onboard XCO.
Do not output reference signal.

1 – Master:
Use onboard XCO.
Output reference signal to slaves using MLVDS.

2 – Slave:
Use external clock reference from MLVDS.Do
not output reference signal.

3 – Slave inline:
Use external clock reference from MLVDS. Output
reference signal to slaves using MLVDS.

4 – Reserved. Do not use.5 –

Reserved. Do not use.

THE DEFAULT STATE IS STANDALONE.

Example:

Input:	$CSS, 1, 3
Output:	$CSS, 1, OK

This configures the clock source to inline slave mode.

Example 2:

Input:	$CSS, 1, 1
Output:	$CSS, 1, OK

This configures the clock source to master mode.