MMIC DIE

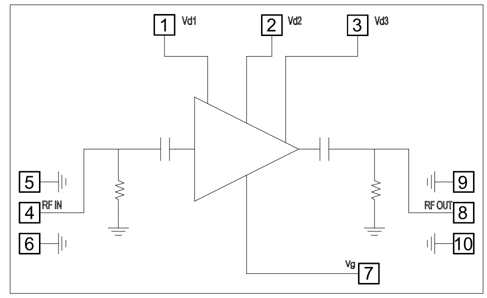
Medium Power Amplifier AVA-17303-D+

50Ω 17 to 31.5 GHz High Linearity Driver

THE BIG DEAL

- High P1dB, Typ. +23.8 dBm
- High OIP3, Typ. +36 dBm
- Supply Voltage, +6 V at 160 mA

FUNCTIONAL DIAGRAM



SEE ORDERING INFORMATION ON THE LAST PAGE

APPLICATIONS

- Test and Measurement Equipment
- Satellite Communications
- Radar, EW, and ECM Defense Systems
- 5G mmWave, MIMO Wireless Infrastructure Systems
- Microwave Radio & VSAT

PRODUCT OVERVIEW

The AVA-17303-D+ is a GaAs MMIC Medium Power Amplifier operating from 17 to 31.5 GHz. This amplifier provides typical 19.2 dB of gain, +23.8 dBm P1dB, and +36 dBm OIP3 while operating from a +6 V power supply at 160 mA. The device is matched to 50Ω and comes as a die suitable for chip and wire assemblies. These characteristics make it ideally suited as a driver amplifier in point-to-point radios and communications systems requiring high output power while maintaining low distortion characteristics.

KEY FEATURES

Features	Advantages
High Gain, Typ. 19.2 dB High P1dB, Typ. +23.8 dBm	High gain and output power make this device excellent for wideband systems from 17 to 31.5 GHz that require at least 0.2 W of operating output power over the full band.
High OIP3, Typ. +36 dBm	High operating OIP3 provides very low in-band distortion products, enabling minimal signal degradation in high fidelity measurement systems and demanding communication systems.
Unpackaged Die	Enables integration into hybrid chip and wire assemblies.

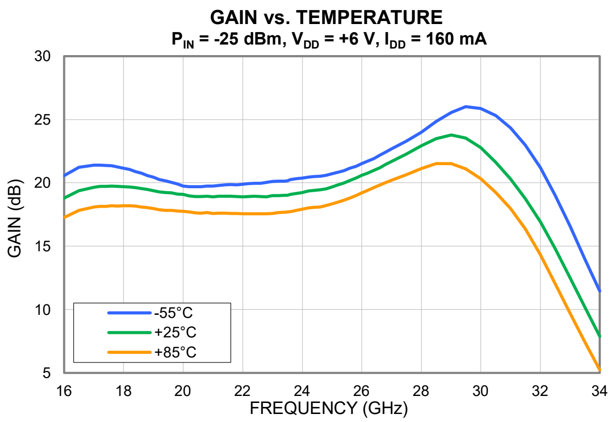
REV. OR
ECO-025192
AVA-17303-D+
MCL NY
250410

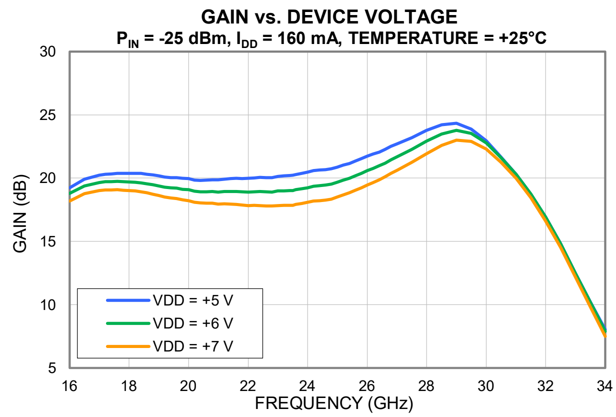
ELECTRICAL SPECIFICATIONS[1] AT +25°C, V_{DD} = +6 V, AND Zo = 50Ω, UNLESS NOTED OTHERWISE

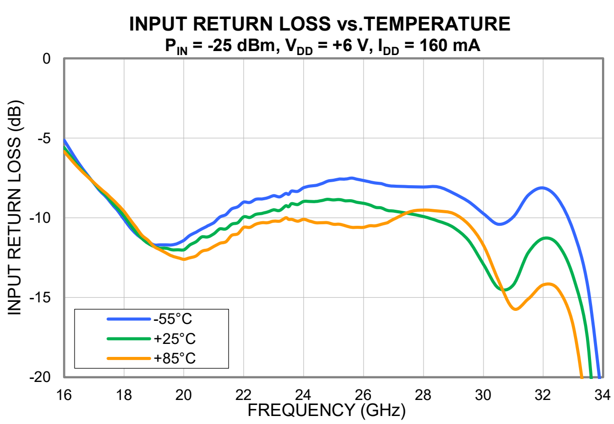
Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency Range		17		31.5	GHz
Gain	17		19.7		dB
	20		19.1		
	24		19.2		
	27		21.7		
	30		22.8		
	31.5		18.7		
Input Return Loss	17		8		dB
	20		12		
	24		9		
	27		10		
	30		13		
	31.5		12		
Output Return Loss	17		14		dB
	20		11		
	24		13		
	27		11		
	30		22		
	31.5		24		
Isolation	17 - 31.5		54		dB
Output Power at 1 dB Compression (P1dB)	17		+23.6		dBm
	20		+23.2		
	24		+23.8		
	27		+25.0		
	30		+23.3		
	31.5		+21.2		
Output Power at Saturation (P_{SAT})[2]	17		+25.3		dBm
	20		+24.5		
	24		+24.5		
	27		+25.2		
	30		+23.6		
	31.5		+21.4		
Output Third-Order Intercept (OIP3) (P_{OUT} = +6 dBm/Tone)	17		+32		dBm
	20		+33		
	24		+36		
	27		+38		
	30		+39		
	31.5		+34		
Noise Figure	17		6.5		dB
	20		4.8		
	24		3.6		
	27		3.0		
	30		3.5		
	31.5		3.8		
Device Operating Voltage (V_{DD})[3]		+5	+6	+7	V
Device Operating Current (I_{DD})[4]			160		mA
Gate Voltage (V_G)			-0.59		V
Gate Current (I_G)[5]			57		µA
Device Current Variation vs. Temperature[6]			-3.6		µA/°C

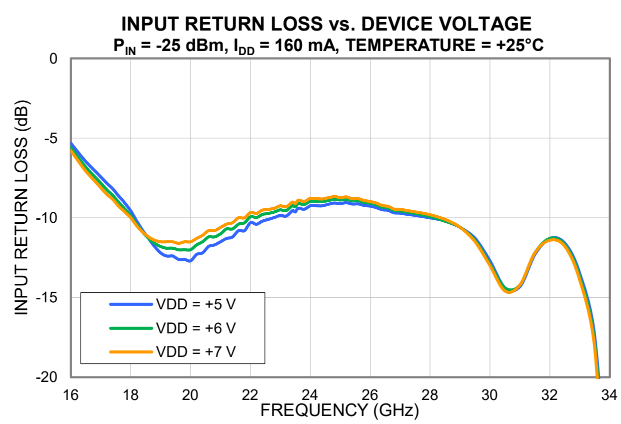
1. Tested in Mini-Circuits Die Characterization Test Board. See Figure 2. Trace and connector losses are de-embedded. Specifications Include the effect of bond wires.
2. Defined as output power at which change is 0.1 per 1 dB change in input power.
3. $V_{DD} = V_{d1} = V_{d2} = V_{d3}$
4. Current at P_{IN} = -25 dBm. Increases to 250 mA at P1dB. $I_{DD} = I_{d1} + I_{d2} + I_{d3}$.
5. Current at P_{IN} = -25 dBm. Increases to 300 µA at P1dB.
6. (Current at +85°C - Current at -55°C)/(140°C). V_G held constant over temperature.

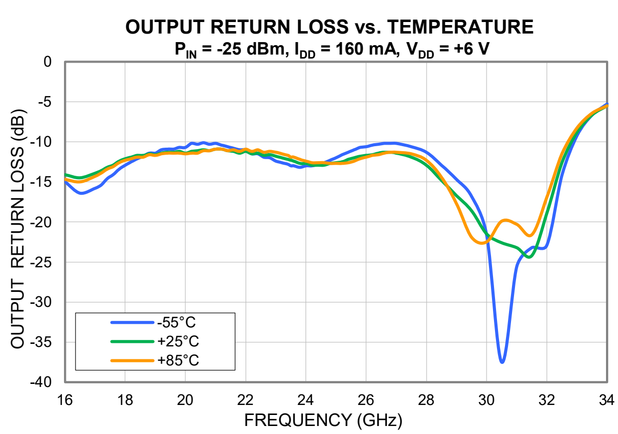
TYPICAL PERFORMANCE GRAPHS

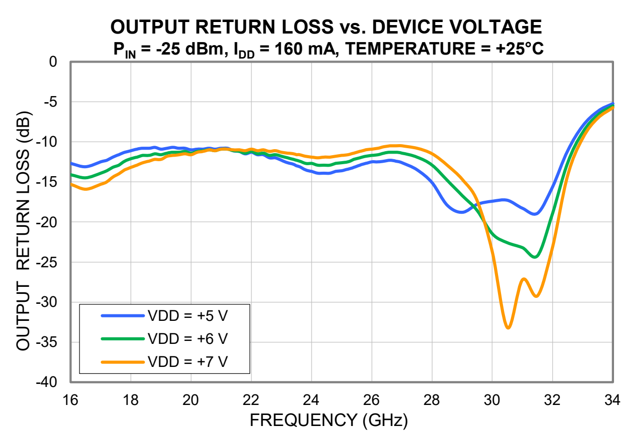




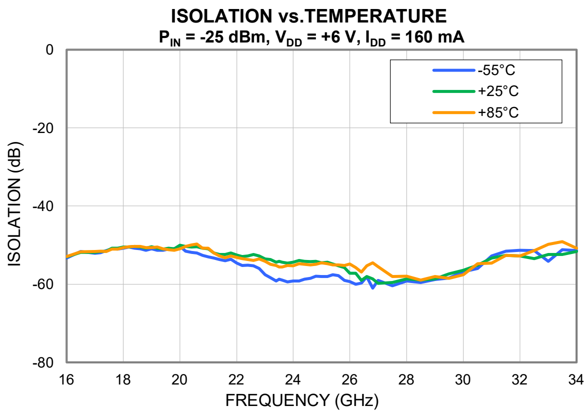


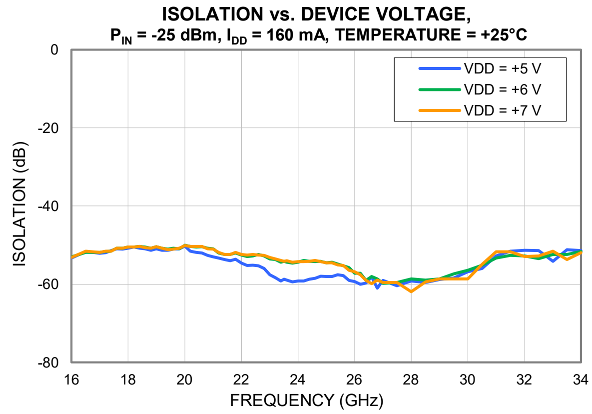


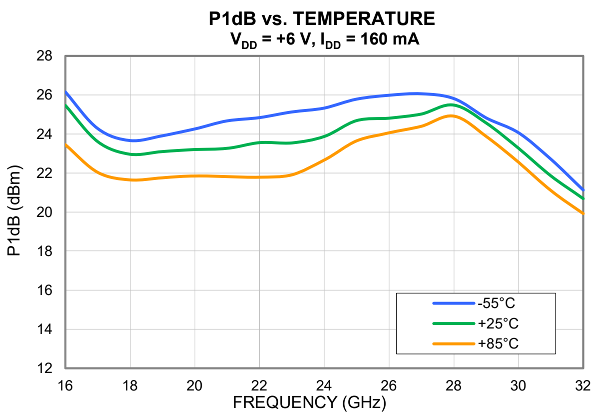


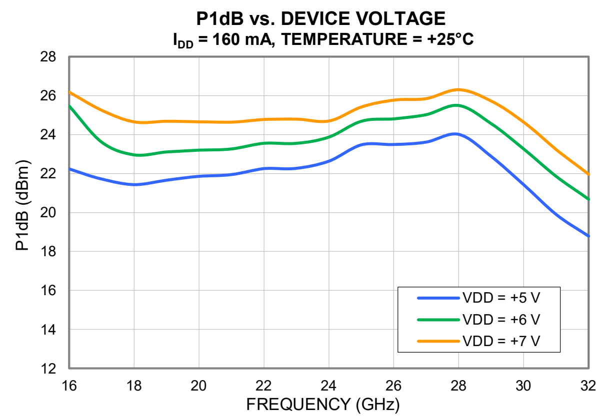


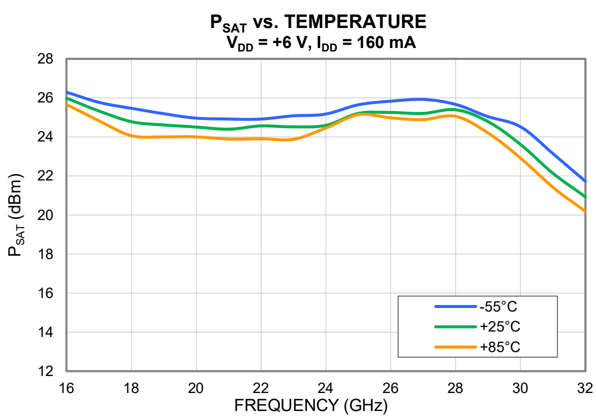
TYPICAL PERFORMANCE GRAPHS

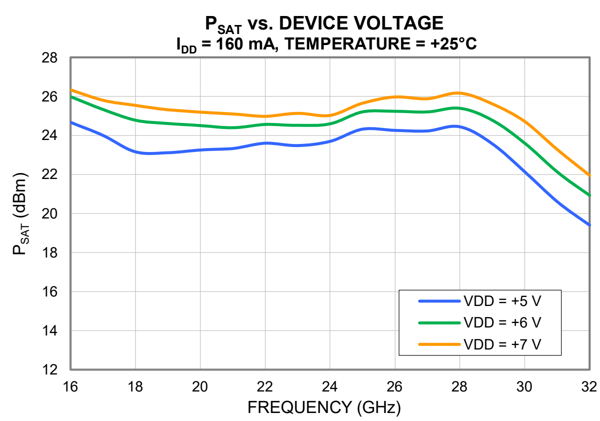






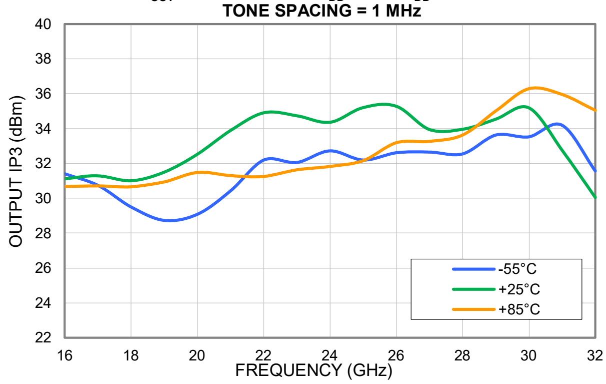




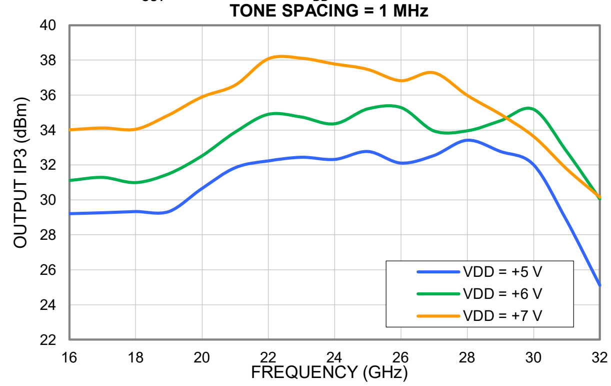


TYPICAL PERFORMANCE GRAPHS

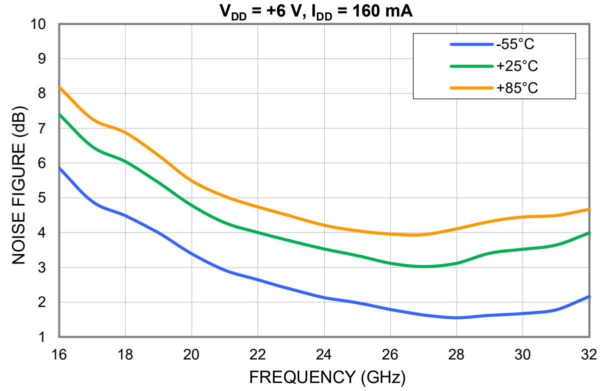
OUTPUT IP3 vs. TEMPERATURE
P_{OUT} = +6 dBm/TONE, V_{DD} = +6 V, I_{DD} = 160 mA
TONE SPACING = 1 MHz



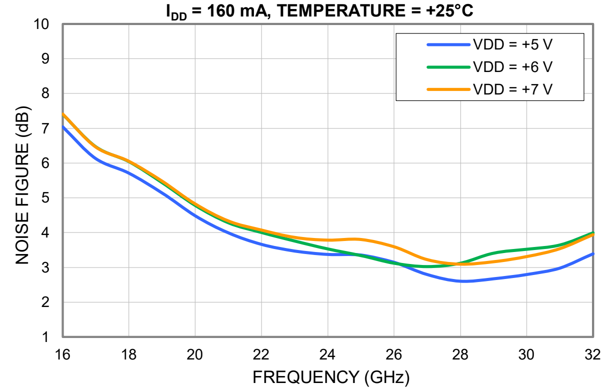
OUTPUT IP3 vs. DEVICE VOLTAGE,
P_{OUT} = +6 dBm/TONE, I_{DD} = 160 mA, TEMP = +25°C
TONE SPACING = 1 MHz



NOISE FIGURE vs. TEMPERATURE
V_{DD} = +6 V, I_{DD} = 160 mA

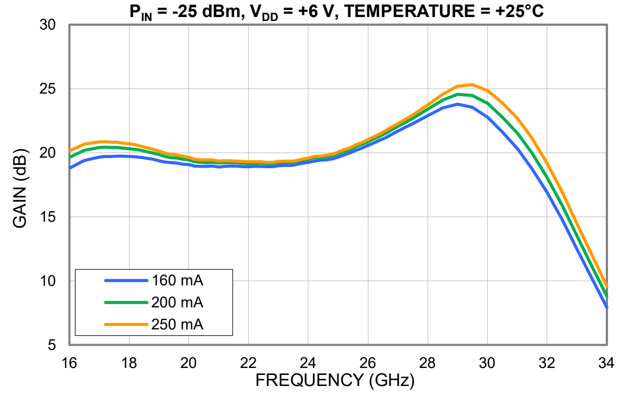


NOISE FIGURE vs. DEVICE VOLTAGE
I_{DD} = 160 mA, TEMPERATURE = +25°C

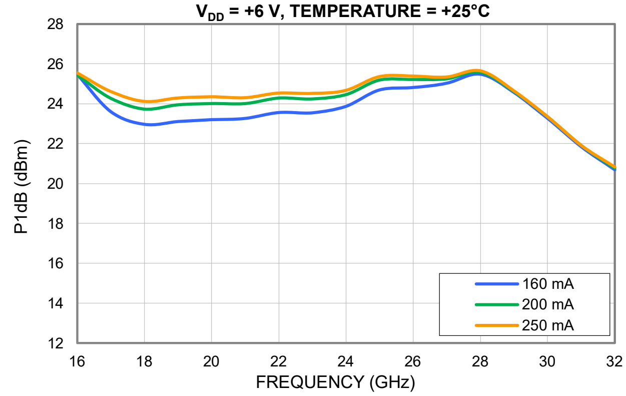


TYPICAL PERFORMANCE GRAPHS

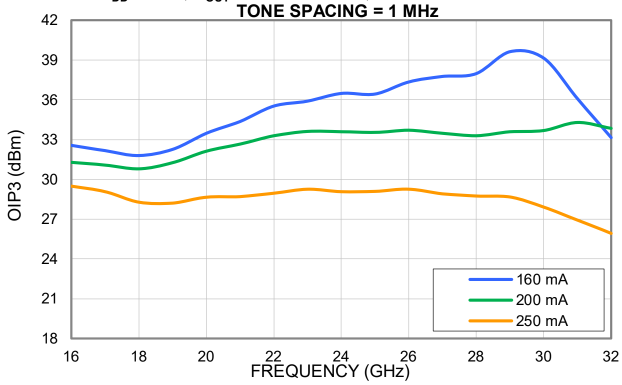
GAIN vs. CURRENT
P_{IN} = -25 dBm, V_{DD} = +6 V, TEMPERATURE = +25°C



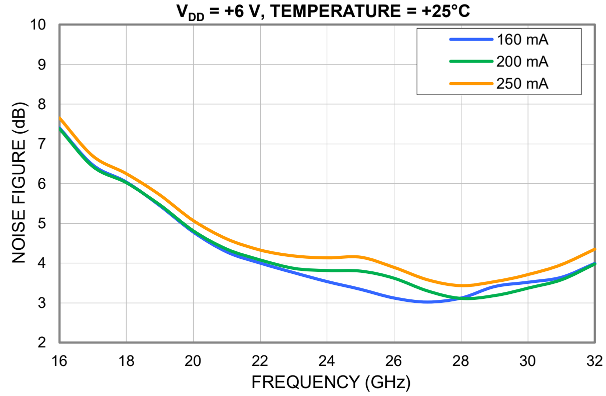
P1dB vs. CURRENT
V_{DD} = +6 V, TEMPERATURE = +25°C



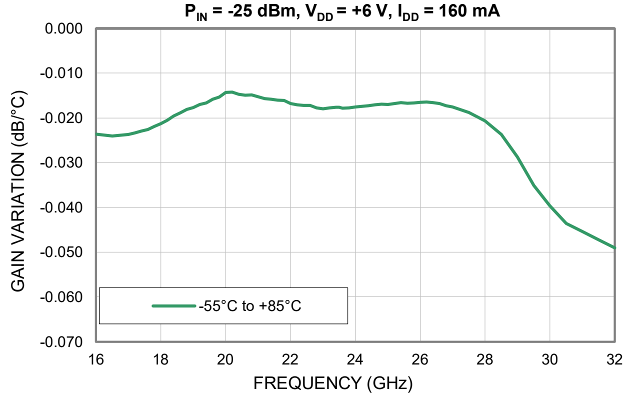
OIP3 vs. CURRENT,
V_{DD} = +6 V, P_{OUT} = +6 dBm/TONE, TEMPERATURE = +25°C
TONE SPACING = 1 MHz



NOISE FIGURE vs. CURRENT,
V_{DD} = +6 V, TEMPERATURE = +25°C



GAIN VARIATION vs. TEMPERATURE
P_{IN} = -25 dBm, V_{DD} = +6 V, I_{DD} = 160 mA



ABSOLUTE MAXIMUM RATINGS[7]

Parameter	Ratings
Operating Temperature[8]	-55°C to +85°C
Storage Temperature[9]	-65°C to +150°C
Junction Temperature[10]	+175°C
Total Power Dissipation	1.8 W
Input Power (CW), V_{DD} = +6 V	+25 dBm
DC Voltage on RF-OUT & V_{DD}[11]	+9 V
DC Drain Current I_{DD}[12]	500 mA
DC Voltage at RF-IN	+9 V
DC Voltage at RF-OUT	+9 V
DC Gate Voltage V_g	-6 V to +1 V
DC Gate Current I_g	8 mA

7. Permanent damage may occur if any of these limits are exceeded. Maximum ratings are not intended for continuous normal operation.
8. Bottom of Die.
9. For die shipped in Gel-Pak see ENV80 (limited by packaging).
10. Peak temperature on Top of Die.
11. $V_{DD} = V_{d1} = V_{d2} = V_{d3}$.
12. $I_{DD} = I_{d1} + I_{d2} + I_{d3}$.

THERMAL RESISTANCE

Parameter	Ratings
Thermal Resistance (Θ_{JC})[13]	46.9°C/W

13. Θ_{JC}= (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

ESD RATING[14]

	Class	Voltage Range	Reference Standard
HBM	1A	250 V to < 500 V	ANSI/ESDA/JEDEC JS-001-2023
CDM	C2A	500 V to < 750 V	ANSI/ESDA/JEDEC JS-002-2022

ESD HANDLING PRECAUTION: This device is designed to be Class 1A for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage.

14. Tested in 4x4mm 20-lead QFN-Style Package

FUNCTIONAL DIAGRAM

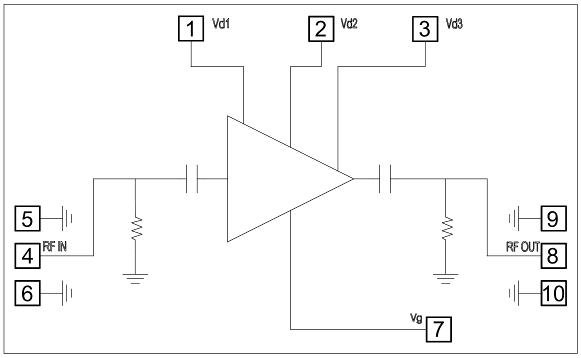


Figure 1. AVA-17303-D+ Functional Diagram

PAD DESCRIPTION

Function	Pad Number	Description (Refer to Fig 1)
RF IN	4	RF Input Port
RF OUT	8	RF Output Port
V_{d1}	1	Drain Voltage Input Port 1
V_{d2}	2	Drain Voltage Input Port 2
V_{d3}	3	Drain Voltage Input Port 3
V_g	7	Gate Voltage Input
GND	5, 6, 9, 10, Bottom of Die	Connected to die backside through vias. Bond wires to ground are optional.

DIE OUTLINE: inches [mm], Typical

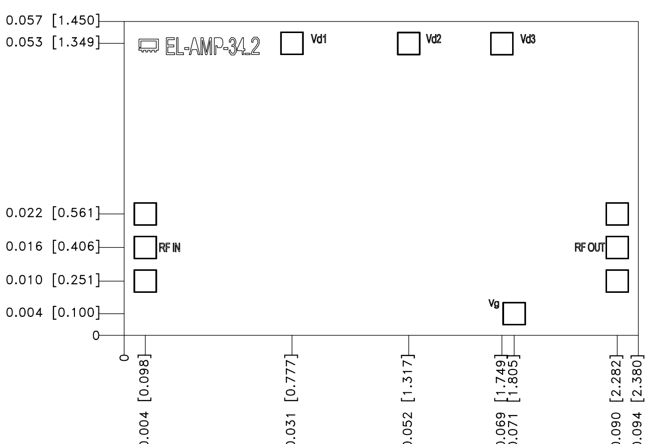


Figure 2. AVA-17303-D+ Die Outline

DIMENSIONS: inches [mm], Typical

Die Size	0.094 x 0.057 [2.38 x 1.45]
Die Thickness	0.0040 [0.100]
Bond Pad Sizes:	0.004 x 0.004 [0.100 x 0.100]
Plating (Pads & Bottom of Die)	Gold

CHARACTERIZATION AND APPLICATION CIRCUIT

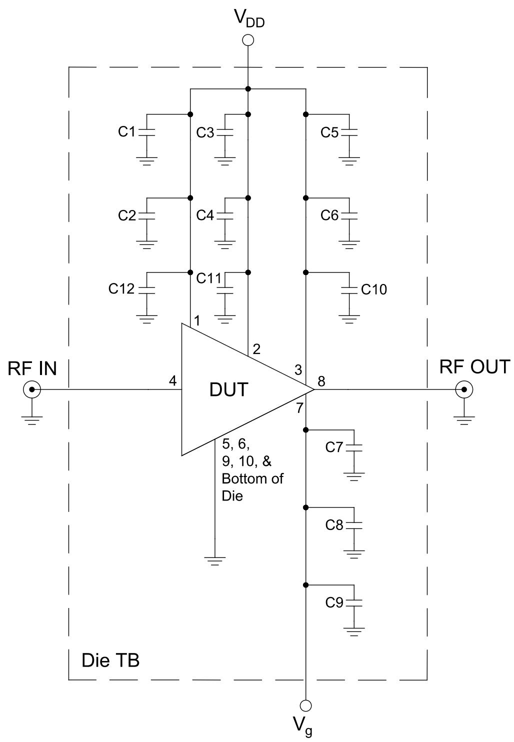


Figure 3. AVA-17303-D+ Evaluation and Application Circuit

Electrical Parameters and Conditions
Gain, Return Loss, Output Power at 1 dB Compression (P1dB), Output IP3 (OIP3), and Noise Figure measured using N5245B PNA-X Microwave Network Analyzer.

Conditions:
1. Gain and Return Loss: P_{IN} = -25 dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, +6 dBm/Tone at output.

Power ON/Power OFF Sequence
Caution: Permanent damage to the device will occur if the Power ON and Power OFF sequences are not followed.

POWER ON:
1. Set V_g = -1.2 V and Turn ON.
2. Set V_{DD} = +6 V and Turn ON.
3. Increase V_g to desired nominal I_{DD} = 160 mA.
4. Turn ON RF signal.

POWER OFF:
1. Turn OFF RF signal.
2. Decrease V_g to -1.2 V
3. Turn OFF V_{DD}
4. Turn OFF V_g

Component	Value	Size	Part Number	Manufacturer
C1, C3, C5, C9	10 µF	1206	CL31B106KBHNNNE	SAMSUNG
C2, C4, C6, C8	0.1 µF	0603	06035C104KAT2A	AVX CORPORATION
C7	100 pF	0603	GRM1885C1H101GA01D	MURATA
C10, C11, C12	100 pF	0.22″ x 0.22″	MA4M3100	MACOM

ASSEMBLY DIAGRAM

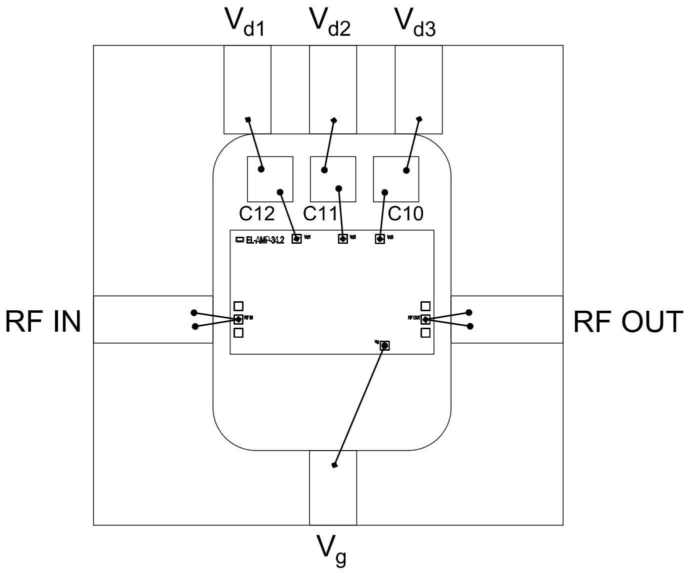


Figure 4. AVA-17303-D+ Assembly Diagram

- Refer to the table in Figure 3. for more details on the passive components
- Bond wire diameter: 1 mil
- Bond wire lengths from Die Pad to PCB at RF IN & RF OUT ports: 18 ± 2 mils
- Bond wire lengths from Die Pad to C10, C11, & C12: 28 ± 2 mils
- Bond wire lengths from C10, C11, & C12 to PCB at V_{d1}, V_{d2}, and V_{d3} ports: 24 ± 2 mils
- Bond wire lengths from Die Pad to PCB at V_g port: 59 ± 2 mils
- Typical Gap from Die edge to PCB edge: 3 mils
- PCB thickness and material: 10 mil Rogers RO4350 (Thickness: 1 oz copper on each side)

ASSEMBLY AND HANDLING PROCEDURE

1. Storage
   Die should be stored in a dry nitrogen purged desiccator or equivalent.
2. ESD Precautions
   MMIC pHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in anti-static protected material, which should be opened only in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
   Devices require careful handling using tools appropriate for manipulating semiconductor chips. It is recommended to handle the chips along the edges with a custom designed collet. The surface of the chip has exposed air bridges and should not be touched with a vacuum collet, tweezers or fingers.
   The die mounting surface must be clean and flat. Using conductive silver-filled epoxy, apply sufficient adhesive to meet the required bond line thickness, fillet height and coverage around the total periphery of the device. The recommended epoxy is Unimec H9890-6A
   or equivalent. Parts should be cured in a nitrogen-filled atmosphere per manufacturer's recommended cure profile.
4. Wire Bonding
   Openings in the surface passivation above the gold bond pads are provided to allow wire bonding to the die. Thermosonic bonding is recommended with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. The suggested interconnect is pure gold, 1 mil diameter wire. Bonds are recommended to be made from the bond pads on the die to the package or substrate. All bond wire length and bond wire height should be kept as short as possible, unless specified by design, to minimize performance degradation due to undesirable series inductance.

ADDITIONAL DETAILED INFORMATION IS AVAILABLE ON OUR DASHBOARD CLICK HERE

Performance Data & Graphs	Data Graphs S-Parameter (S2P Files) Data Set (.zip file)	
Case Style	Die	
RoHS Status	Compliant	
Die Ordering and Packaging Information	Quantity, Package	Model No.
	Gel - Pak: 5, 10, 50, 100 KGD*	AVA-17303-DG+
	Medium†, Partial wafer: KGD*<630	AVA-17303-DP+
	Full wafer†	AVA-17303-DF+
	†Available upon request contact sales representative. Refer to AN-60-067	
Die Marking	EL-AMP-34_2	
Environmental Ratings	ENV80	

* Known Good Die ("KGD") means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within a predefined range. While DC testing is not definitive, it does provide a high degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.