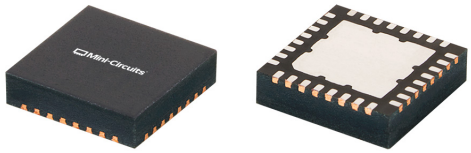
MMIC SURFACE MOUNT

Medium Power Amplifier AVA-6183MP+

50Ω 6 to 18 GHz Dual Biased

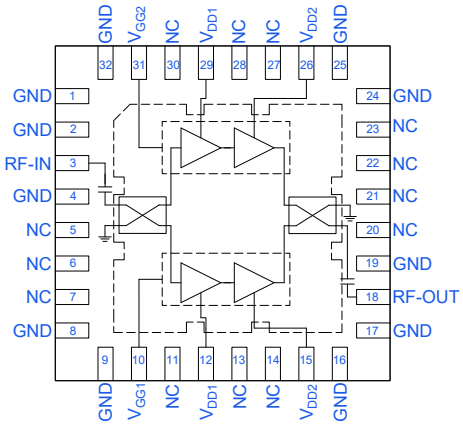
THE BIG DEAL

- High Saturated Output Power, Typ. +30.9 dBm
- High Gain, Typ. 19.3 dB
- High OIP3, Typ. +35.5 dBm
- Supply Voltage +6 V
- 5x5 mm 32-Lead QFN-Style Package



Generic photo used for illustration purposes only

FUNCTIONAL DIAGRAM (Top View)



APPLICATIONS

- Microwave Radio Backhaul Systems
- Radar, EW, and ECM Defense Systems
- Satellite Communications
- Test and Measurement Equipment

PRODUCT OVERVIEW

Mini-Circuits' AVA-6183MP+ is a wideband, medium power MMIC amplifier fabricated on a GaAs pHEMT process with high output power and broadband gain. Operating from 6 to 18 GHz, this amplifier features typical +27.9 dBm P1dB, +30.9 dBm P_{SAT}, and 19.3 dB gain while operating from a +6 V power supply. AVA-6183MP+ is internally matched to 50 Ohms and comes in a 5x5 mm 32-Lead QFN-style package. These characteristics make it the ideal driver amplifier for a wide range of applications.

KEY FEATURES

Features	Advantages
High Gain, Typ. 19.3 dB	The MMIC amplifier's high gain enables fewer system components in transmit and receive signal chains.
High Saturated Output Power, Typ. +30.9 dBm	High saturated output power makes this amplifier ideal as a driver amplifier in 5G MIMO, backhaul radio, satellite communication, and Electronic Warfare applications.
Dual bias offering gate and drain supply voltage control	Offers control over operating point for improved linearity and higher power-added efficiency. Gate bias may be used to support power control or shutdown functionality.
5x5 mm 32-Lead QFN-Style Package	Small footprint saves space in dense layouts while providing low inductance, repeatable transitions, and excellent thermal contact to the PCB. Industry standard packaging allows for ease of assembly in high volume manufacturing processes.

REV. OR
ECO-027042
AVA-6183MP+
MCL NY
250919

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ELECTRICAL SPECIFICATIONS[1] AT +25°C, V_{DD} = +6 V, I_{DD} = 550 mA, AND Z_O = 50Ω UNLESS NOTED OTHERWISE

Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency Range		6		18	GHz
Gain	6	16.7	19.9		dB
	9	16.2	20.0		
	12	14.9	19.3		
	15	15.1	19.8		
	18	14.5	20.1		
Input Return Loss	6		18		dB
	9		16		
	12		12		
	15		20		
	18		14		
Output Return Loss	6		17		dB
	9		15		
	12		16		
	15		19		
	18		15		
Isolation	6-18		60.6		dB
Output Power at 1 dB Compression (P1dB)	6		+26.5		dBm
	9		+28.8		
	12		+27.9		
	15		+28.1		
	18		+29.0		
Output Power at Saturation (P_{SAT})[2]	6		+29.4		dBm
	9		+31.0		
	12		+30.9		
	15		+31.1		
	18		+29.8		
Output Third-Order Intercept (OIP3) (P_{OUT} = +16 dBm/Tone)	6		+32.8		dBm
	9		+34.1		
	12		+35.5		
	15		+35.3		
	18		+33.8		
Noise Figure	6		7.7		dB
	9		5.1		
	12		4.8		
	15		4.8		
	18		5.1		
Device Operating Voltage (V_{DD})[3,4]		+5	+6	+7	V
Device Operating Current (I_{DD})[5,6]		220	550	600	mA
Device Operating Gate Voltage (V_{GG})[7,8]			-0.78		V
Device Operating Gate Current (I_{GG})[9]			0.79		mA
Device Current Variation Vs. Temperature[10]			-0.435		mA/°C
Device Current Variation Vs. Voltage[11]			+0.094		mA/mV

1. Tested on Mini-Circuits Characterization Test Board TB-AVA-6183MPC+. See Figure 2. De-embedded to the device reference plane.
2. Defined as output power at which change is 0.1 dB per 1 dB change in input power.
3. $V_{DD} = V_{DD1} = V_{DD2}$
4. Voltage must be applied to all V_{DD1} and V_{DD2} pins for standard operation.
5. Current at P_{IN} = -25 dBm. Increases to 1250 mA at P_{SAT}.
6. $I_{DD} = I_{DD1} + I_{DD2}$
7. $V_{GG} = V_{GG1} = V_{GG2}$
8. Voltage must be applied to both V_{GG1} and V_{GG2} pins for standard operation.
9. $I_{GG} = I_{GG1} + I_{GG2}$
10. (Current at +85°C - Current at -55°C)/(+85°C - -55°C)
11. (Current at +7 V - Current at +5 V)/(+7 V - +5 V)

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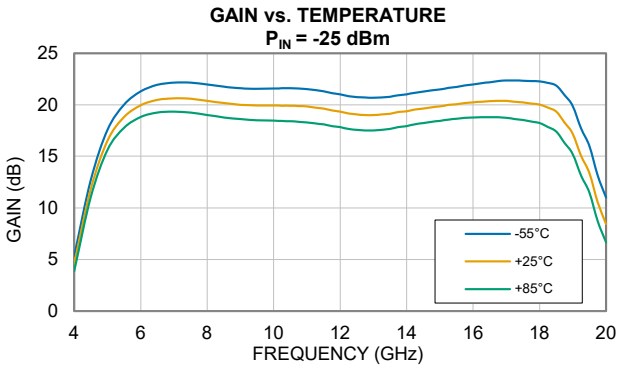
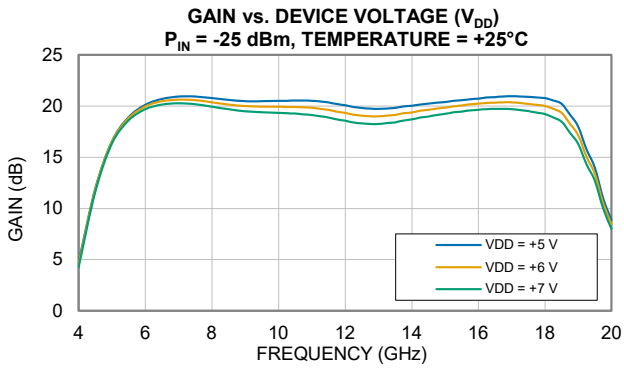
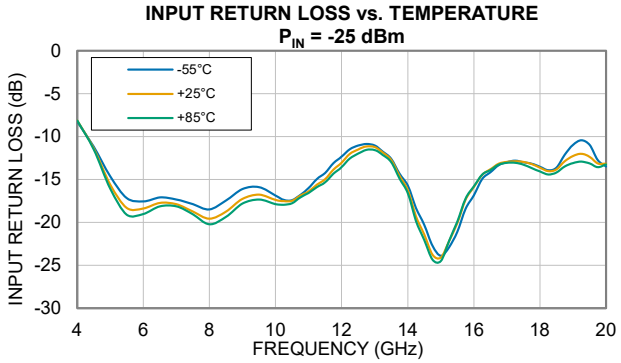
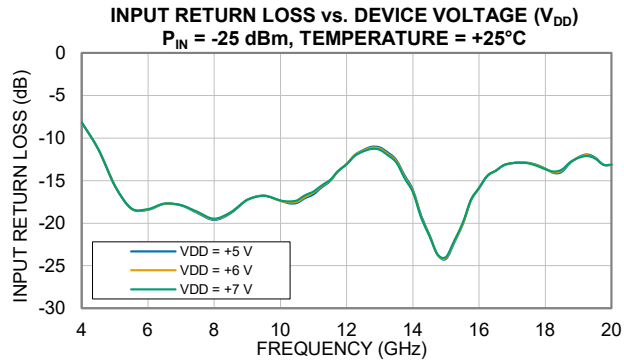
TYPICAL PERFORMANCE GRAPHS

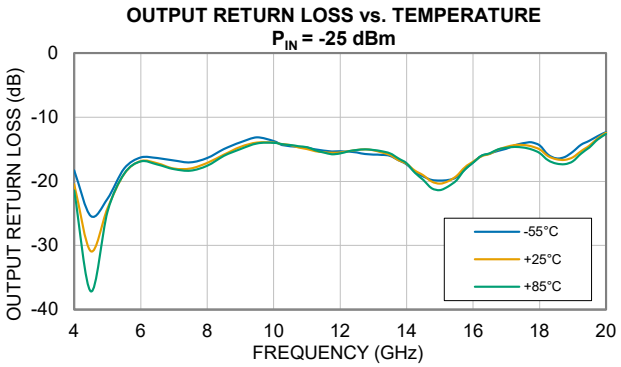
Note: Data over temperature was taken at V_{DD} = +6 V. For over temperature data, V_{GG} was adjusted until I_{DD} = 550 mA at all temperatures specified. For over voltage data, V_{GG} was adjusted until I_{DD} = 550 mA at all V_{DD} levels specified. For additional data over additional current levels at specified voltages, see the View Data page of the model dashboard.

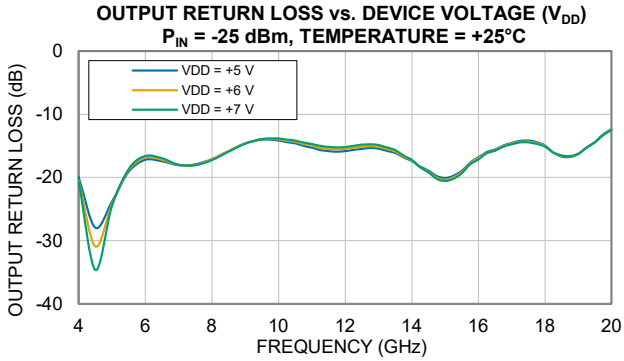












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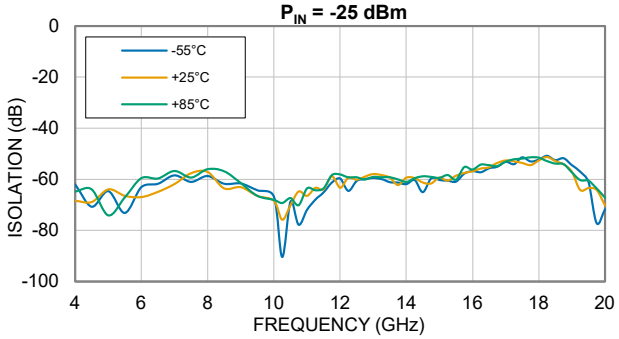
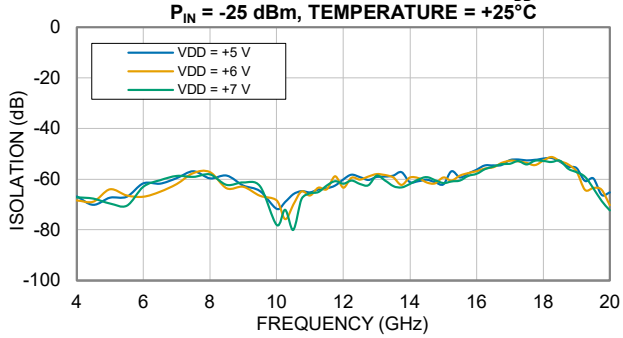
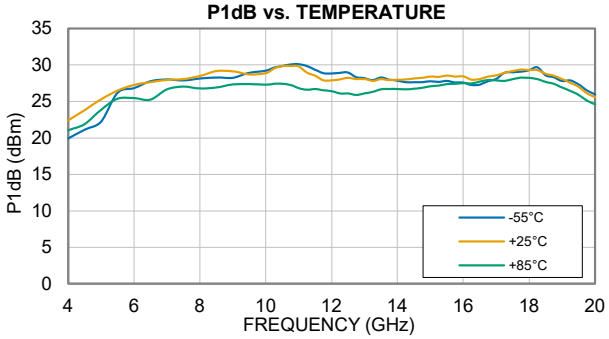
ISOLATION vs. TEMPERATURE
P_{IN} = -25 dBm



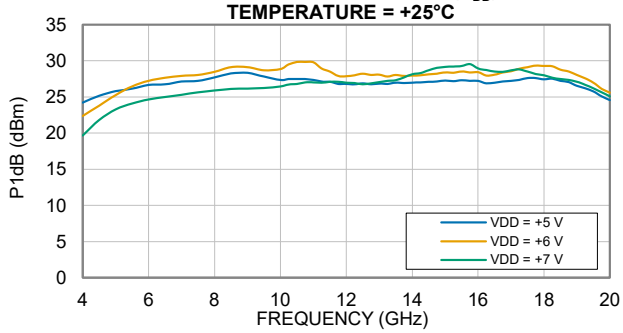
ISOLATION vs. DEVICE VOLTAGE (V_{DD})
P_{IN} = -25 dBm, TEMPERATURE = +25°C



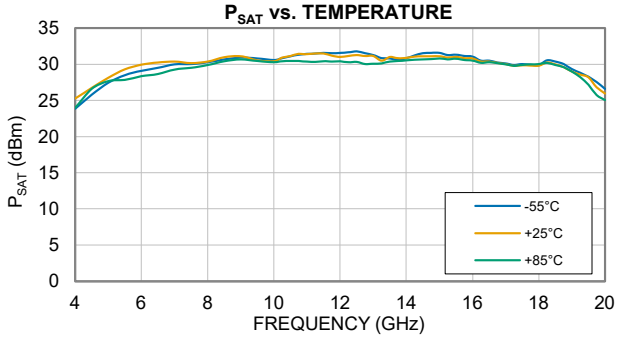
P1dB vs. TEMPERATURE



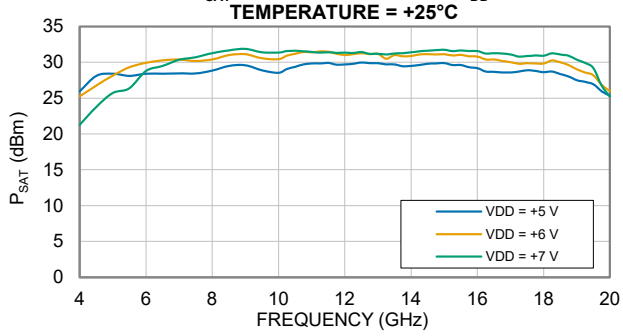
P1dB vs. DEVICE VOLTAGE (V_{DD})
TEMPERATURE = +25°C



P_{SAT} vs. TEMPERATURE



P_{SAT} vs. DEVICE VOLTAGE (V_{DD})
TEMPERATURE = +25°C



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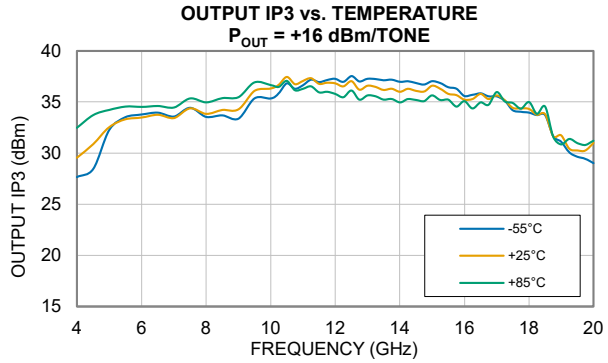

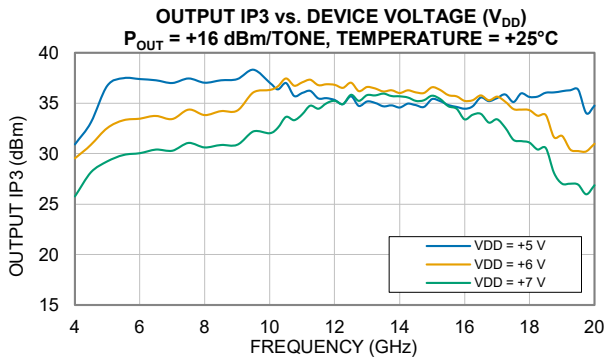

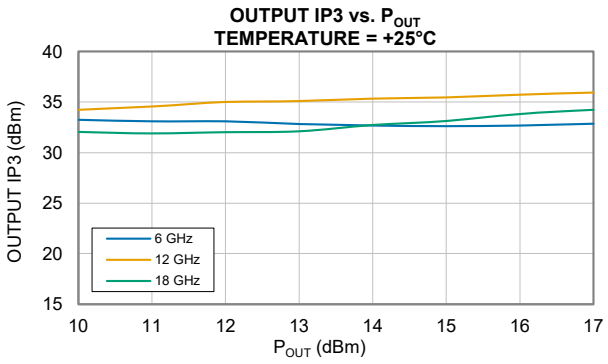

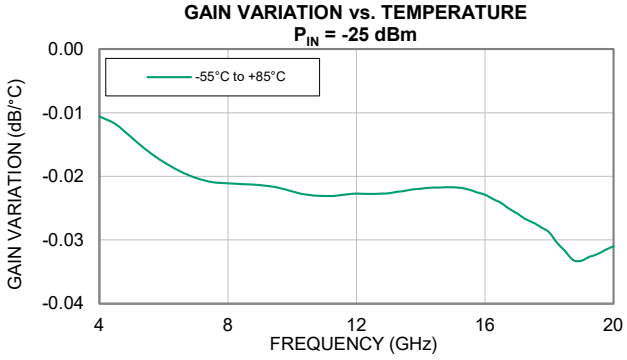

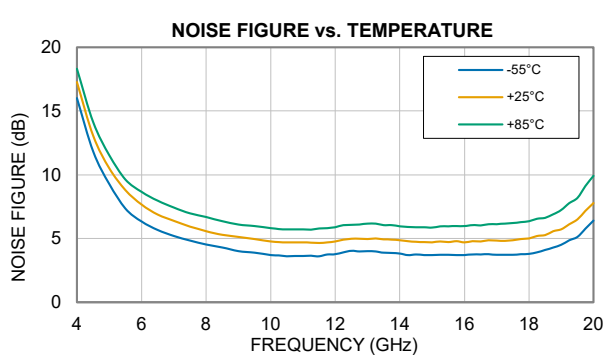

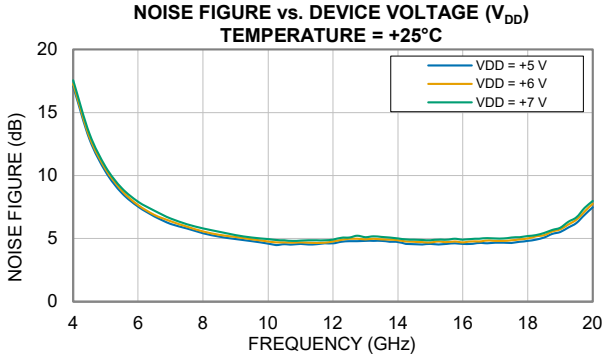

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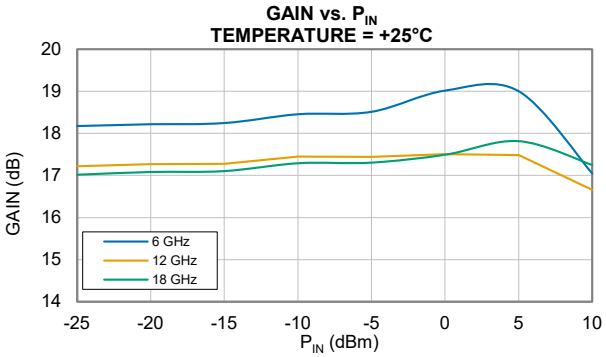

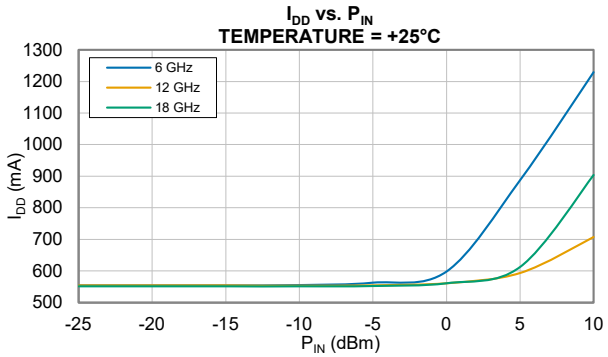

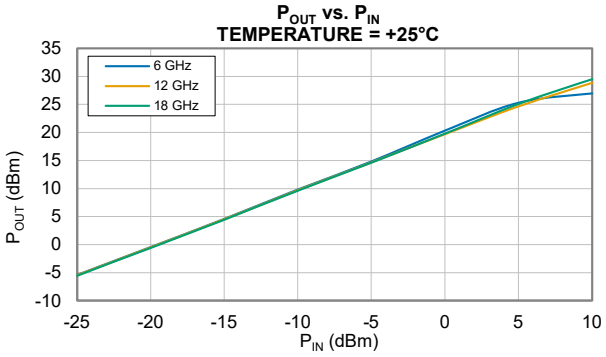

ABSOLUTE MAXIMUM RATINGS[12]

Parameter	Ratings
Operating Temperature	-55°C to +85°C
Storage Temperature	-65°C to +150°C
Total Power Dissipation	6.5 W
Junction Temperature[13]	+175°C
Input Power (CW), V_{DD}[14] = +6 V	+26 dBm
DC Voltage on RF-OUT	+10 V
DC Voltage on RF-IN	+10 V
DC Drain Voltage on V_{DD}	+7.5 V
DC Drain Current I_{DD}[15]	1400 mA
DC Gate Voltage on V_{GG}[16]	-3 V < V_{GG} < 0 V
DC Gate Current I_{GG}[17]	5 mA

12. Permanent damage may occur if any of these limits are exceeded. Maximum ratings are not intended for continuous normal operation.
13. Peak temperature on top of die.
14. $V_{DD} = V_{DD1} = V_{DD2}$
15. $I_{DD} = I_{DD1} + I_{DD2}$
16. $V_{GG} = V_{GG1} = V_{GG2}$
17. $I_{GG} = I_{GG1} + I_{GG2}$

THERMAL RESISTANCE

Parameter	Ratings
Thermal Resistance (Θ_{JC})[18]	18.3°C/W

18. Θ_{JC}= (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

ESD RATING

	Class	Voltage Range	Reference Standard
Human Body Model (HBM)	1A	250 V < 500 V	ANSI/ESDA/JEDEC JS-001-2023
Charged Device Model (CDM)	C3	> 1000 V	ANSI/ESDA/JEDEC JS-002-2022

ESD HANDLING PRECAUTION: This device is designed to be Class 1A for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage.

MSL RATING

Moisture Sensitivity: MSL3 in accordance with IPC/JEDEC J-STD-020E/JEDEC J-STD-033C

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FUNCTIONAL DIAGRAM (TOP VIEW)

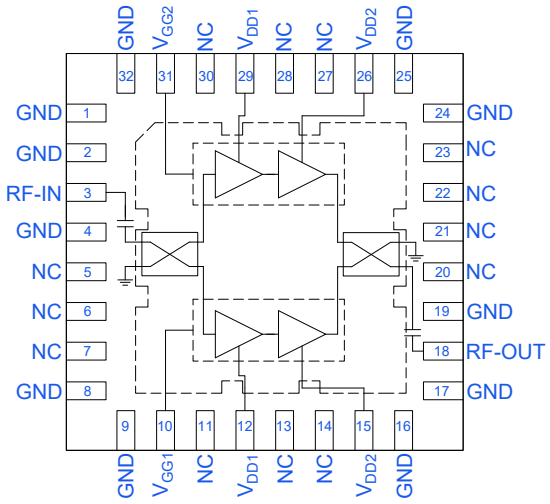

Figure 1. AVA-6183MP+ Functional Diagram

PAD DESCRIPTION

Function	Pad Number	Description (Refer to Figure 2)
RF-IN	3	RF-IN pad connects to RF-Input port.
RF-OUT	18	RF-OUT pad connects to RF-Output port.
V_{DD1}	12, 29	DC Input pads connects to voltage input ports, V_{DD1}.
V_{DD2}	15, 26	DC Input pads connects to voltage input ports, V_{DD2}.
V_{GG1}	10	DC Input pads connects to voltage input ports, V_{GG1}.
V_{GG2}	31	DC Input pads connects to voltage input ports, V_{GG2}.
GND	1, 2, 4, 8, 9, 16, 17, 19, 24, 25, 32, & Paddle	Connects to ground.
NC	5-7, 11, 13, 14, 20-23, 27, 28, 30	Not used internally. Connected to ground on test board.

EVALUATION BOARD

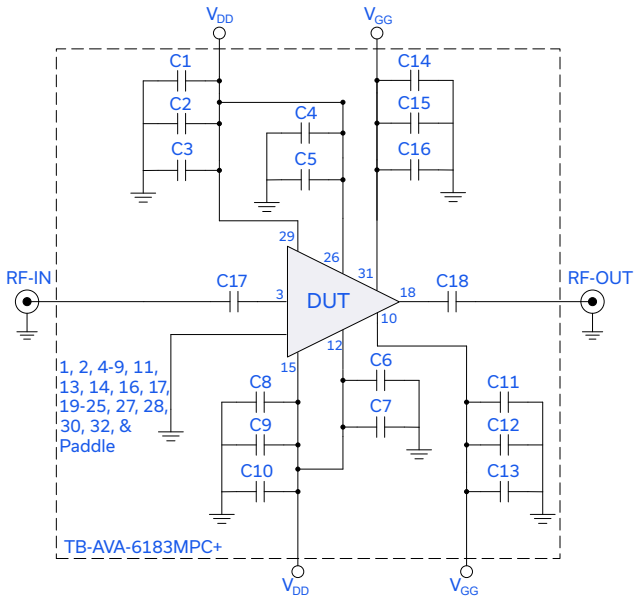

Figure 2. AVA-6183MP+ Evaluation and Application Circuit

Electrical Parameters and Conditions
Gain, Return Loss, Output Power at 1 dB Compression (P1dB), Output Power at Saturation (P_{SAT}), Output IP3 (OIP3), and Noise Figure measured using N52425B PNA-X Microwave Network Analyzer.

Conditions:
1. Gain and Return Loss: P_{IN} = -25 dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, +16 dBm/tone at output.

Power ON/Power OFF Sequence:
Caution: Permanent damage to the device will occur if the Power ON and Power OFF sequences are not followed.

Power ON:
1) Set V_{GG} = -2 V. Apply V_{GG}.
2) Set V_{DD} = +6 V. Apply V_{DD}.
3) Increase V_{GG} to obtain the desired I_{DD} as shown in specification table.
4) Apply RF Signal.

Power OFF:
1) Turn off RF Signal.
2) Adjust V_{GG} to -2 V.
3) Turn off V_{DD}.
4) Turn off V_{GG}.

Component	Value	Size	Part Number	Manufacturer
C3, C5, C6, C8, C11, & C16	100 pF	0603	GRM1885C1H101GA01D	Murata
C2, C4, C7, C9, C12, &C15	0.01 µF	0402	GRM155R71E103KA01D	Murata
C1, C10, C13, & C14	10 µF	1206	CL31B106KBHNNNE	Samsung
C17 & C18	30 pF	0201	P21BNL300M5ST	KDL

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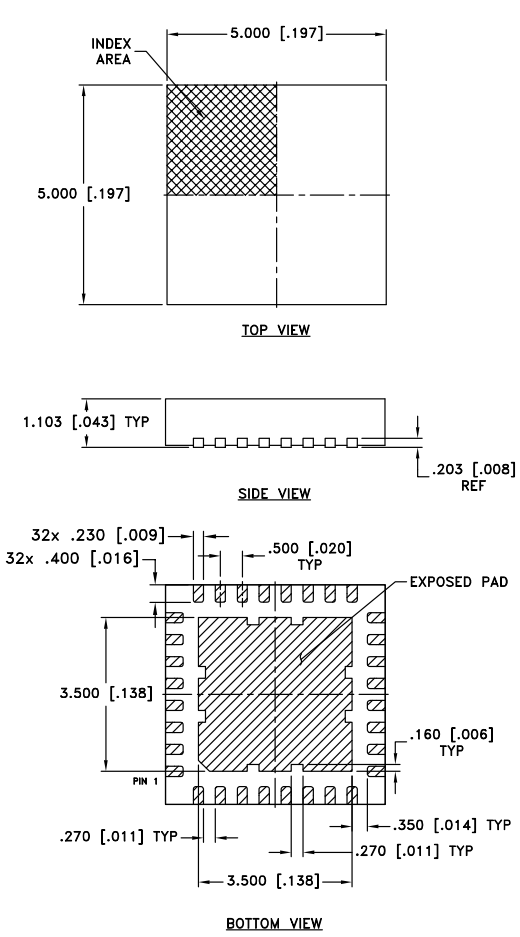
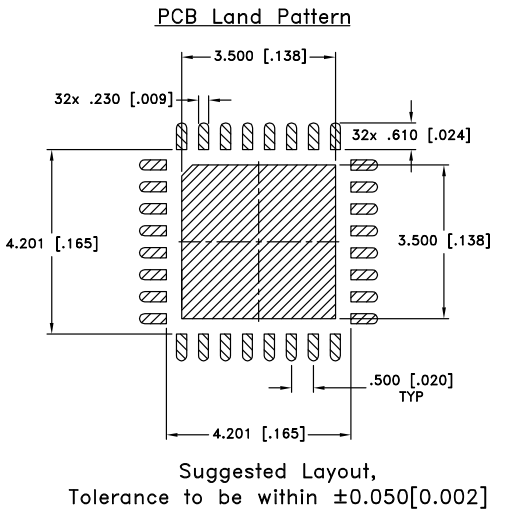
CASE STYLE DRAWING

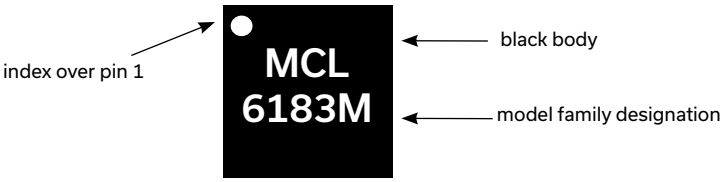




Weight: .056 Grams

Dimensions are in mm [Inches]. Tolerances: 2 Pl. ± 0.254 [0.01]; 3 Pl. ± 0.127 [0.005] mm [inches]

PRODUCT MARKING



Marking may contain other features or characters for internal lot control

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ADDITIONAL DETAILED INFORMATION IS AVAILABLE ON OUR DASHBOARD CLICK HERE

Performance Data & Graphs	Data Graphs S-Parameter (S2P Files) Data Set (.zip file)
Case Style	DG1677-8. QFN-style package, exposed paddle, Lead Finish: Nickel Palladium Gold
RoHs Status	Compliant
Tape & Reel **Standard quantities available on reel**	F102 7″ reels with 20, 50, 100, 200, or 500 devices 13″ 1,000 devices
Suggested Layout for PCB Design	PL-833
Evaluation Board	TB-AVA-6183MPC+ Gerber File
Environmental Ratings	ENV08T10
Product Handling	The use of no-clean solder is recommended. This package cannot be subjected to aqueous wash.

NOTES

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the standard terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/terms/viewterm.html