MMIC DIE

Medium Power Amplifier AVA-6183MP-D+

50Ω 6 to 18 GHz Dual Bias

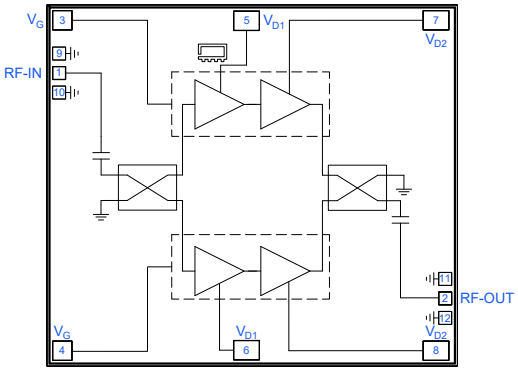
THE BIG DEAL

- High Saturated Output Power, Typ. +30.3 dBm
- High Gain, Typ. 19.1 dB
- High OIP3, Typ. +37.2 dBm
- Supply Voltage +6 V

APPLICATIONS

- Microwave Radio Backhaul Systems
- Radar, EW, and ECM Defense Systems
- Satellite Communication
- Test and Measurement Equipment

FUNCTIONAL DIAGRAM



SEE ORDERING INFORMATION ON THE LAST PAGE

PRODUCT OVERVIEW

Mini-Circuits' AVA-6183MP-D+ is a wideband, medium power MMIC amplifier fabricated on a GaAs pHEMT process with high output power and broadband gain. Operating from 6 to 18 GHz, this amplifier features typical +27.3 dBm P1dB, +30.3 dBm $P_{SAT,}$ and 19.1 dB Gain while operating from a +6 V power supply. AVA-6183MP-D+ is internally matched to 50 Ohms and measures only 2.81x3.2 mm. These characteristics make it the ideal driver amplifier for a wide range of applications including back haul radio, radar and satellite communications.

KEY FEATURES

Feature	Advantages
High Gain, Typ. 19.1 dB	The MMIC amplifier's high gain enables fewer system components in receiver signal chains.
High Saturated Output Power, Typ. +30.3 dBm	High saturated output power and high gain make this amplifier ideal as a driver amplifier in backhaul radio, satellite communication, and EW applications.
Dual bias offering gate and drain supply voltage control	Offers control over operating point for improved linearity, and higher power-added efficiency. Gate bias may be used to support power control or shutfown functionality.
Unpackaged Die	Suitable for chip and wire hybrid assemblies.

REV. OR
ECO-027070
AVA-6183MP-D+
MCL NY
250922

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ELECTRICAL SPECIFICATIONS[1] AT +25°C, V_{DD} = +6 V, I_{DD} = 550 mA, AND Z_O = 50Ω UNLESS NOTED OTHERWISE

Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency Range		6		18	GHz
Gain	6		19.4		dB
	9		19.7		
	12		19.1		
	15		19.6		
	18		20.2		
Input Return Loss	6		17		dB
	9		17		
	12		12		
	15		20		
	18		18		
Output Return Loss	6		18		dB
	9		15		
	12		19		
	15		20		
	18		20		
Isolation	6-18		56.8		dB
Output Power at 1 dB Compression (P1dB)	6		+25.4		dBm
	9		+28.4		
	12		+27.3		
	15		+27.4		
	18		+28.8		
Output Power at Saturation (P_{SAT})[2]	6		+28.3		dBm
	9		+30.2		
	12		+30.3		
	15		+31.0		
	18		+30.0		
Output Third-Order Intercept (OIP3) (P_{OUT} = +16 dBm/Tone)	6		+32.4		dBm
	9		+35.2		
	12		+37.2		
	15		+36.4		
	18		+36.2		
Noise Figure	6		7.9		dB
	9		5.4		
	12		5.0		
	15		4.8		
	18		4.9		
Device Operating Voltage (V_{DD})[3,4]		+5	+6	+7	V
Device Operating Current (I_{DD})[5,6]		220	550	600	mA
Device Operating Gate Voltage (V_{GG})[7, 8]			-0.78		V
Device Operating Gate Current (I_{GG})[9]			0.79		mA
Device Current Variation Vs. Temperature[10]			-0.435		mA/°C
Device Current Variation Vs. Voltage[11]			+0.094		mA/mV

1. Tested on Mini-Circuits Die Characterization Test Board. See Figure 3. Loss de-embedded to the RF input and output wire bonds of the device.
2. Defined as output power at which change is 0.1 dB per 1 dB change in input power.
3. $V_{DD} = V_{D1} = V_{D2}$
4. Voltage must be applied to all V_{D1} and V_{D2} pins for standard operation.
5. Current at P_{IN} = -25 dBm. Increases to 1250 mA at P_{SAT}.
6. I_{DD} is the sum of the current of the I_{D1} and I_{D2} pads.
7. $V_{GG} = V_G$
8. Voltage must be applied to both V_G pads for standard operation.
9. I_{GG} is the sum of the current of the I_G pads.
10. (Current at +85°C - Current at -55°C)/(+85°C - -55°C)
11. (Current at +7 V - Current at +5 V)/(+7 V - +5 V)

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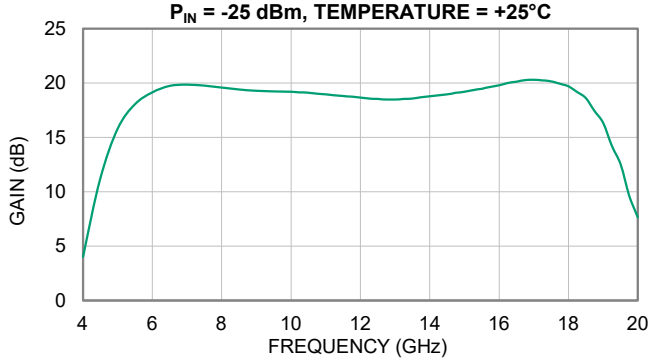
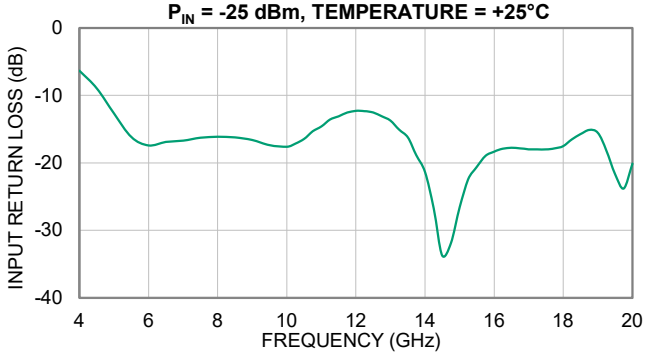
TYPICAL PERFORMANCE GRAPHS

Note: All data taken at V_{DD} = +6 V. At +25°C, V_{GG} has been adjusted to achieve I_{DD} = 550 mA. For over voltage, current, and temperature data, see AVA-6183MP+.

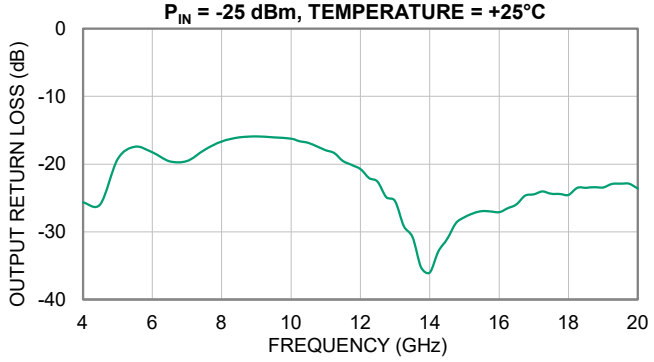
GAIN vs. FREQUENCY
P_{IN} = -25 dBm, TEMPERATURE = +25°C



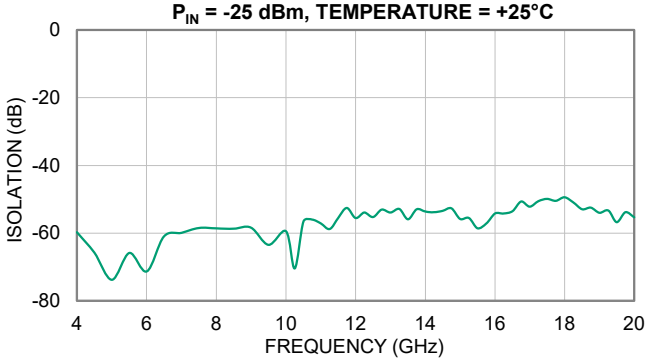
INPUT RETURN LOSS vs. FREQUENCY
P_{IN} = -25 dBm, TEMPERATURE = +25°C



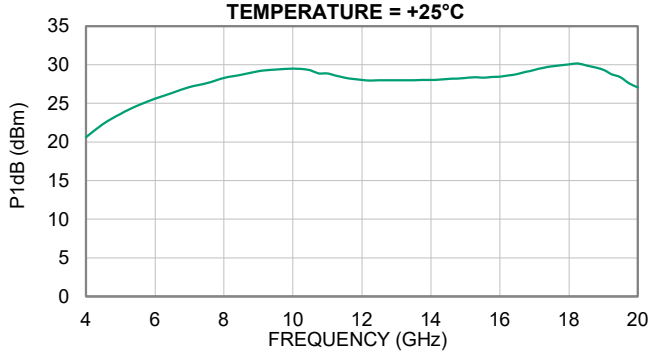
OUTPUT RETURN LOSS vs. FREQUENCY
P_{IN} = -25 dBm, TEMPERATURE = +25°C



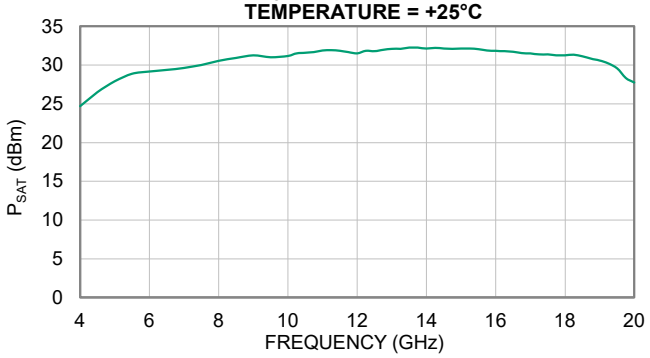
ISOLATION vs. FREQUENCY
P_{IN} = -25 dBm, TEMPERATURE = +25°C



P1dB vs. FREQUENCY
TEMPERATURE = +25°C



P_{SAT} vs. FREQUENCY
TEMPERATURE = +25°C



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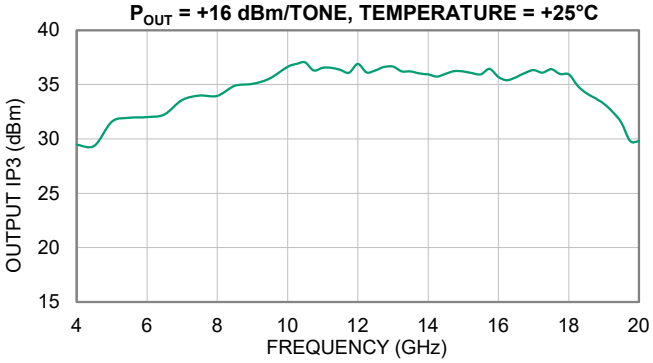
50Ω 6 to 18 GHz Dual Bias

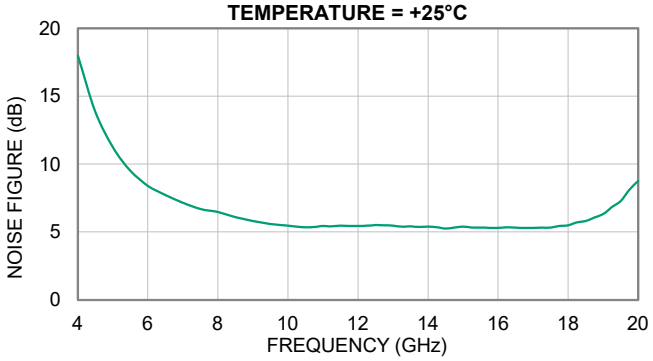
TYPICAL PERFORMANCE GRAPHS

Note: All data taken at V_{DD} = +6 V. At +25°C, V_{GG} has been adjusted to achieve I_{DD} = 550 mA. For over voltage, current, and temperature data, see AVA-6183MP+.

OUTPUT IP3 vs. FREQUENCY
P_{OUT} = +16 dBm/TONE, TEMPERATURE = +25°C



NOISE FIGURE vs. FREQUENCY
TEMPERATURE = +25°C



Medium Power Amplifier AVA-6183MP-D+

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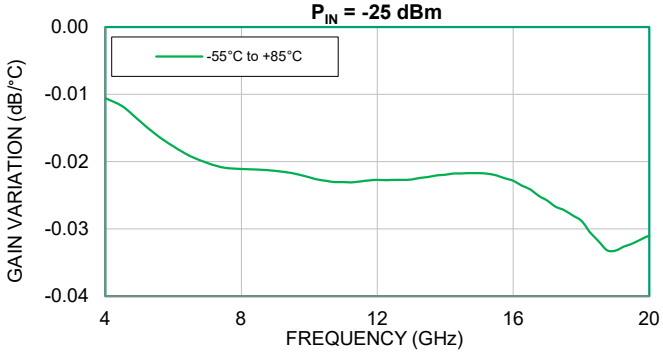
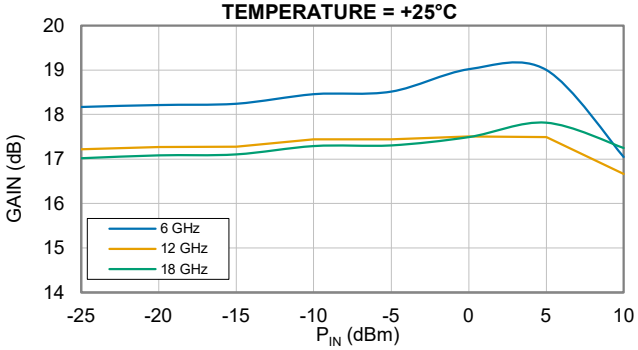
TYPICAL PERFORMANCE GRAPHS

Note: All data taken in this section represents the Die attached in a 5x5 mm 32-Lead QFN-style package and measured on Mini-Circuits Characterization Test Board TB-AVA-6183MPC+. All data taken at V_{DD} = +6 V. At +25°C, V_{GG} has been adjusted to achieve I_{DD} = 550 mA. For over voltage, current, and temperature data, see AVA-6183MP+.

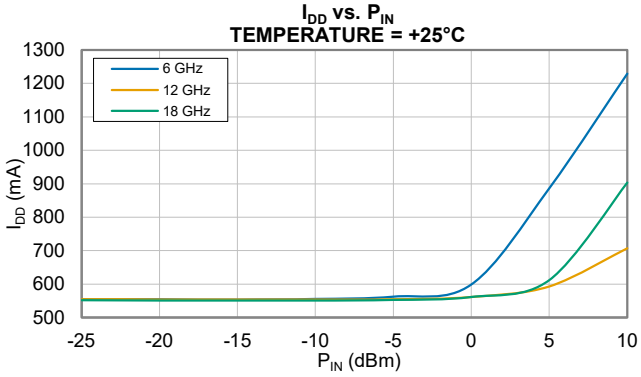
GAIN VARIATION vs. TEMPERATURE
P_{IN} = -25 dBm



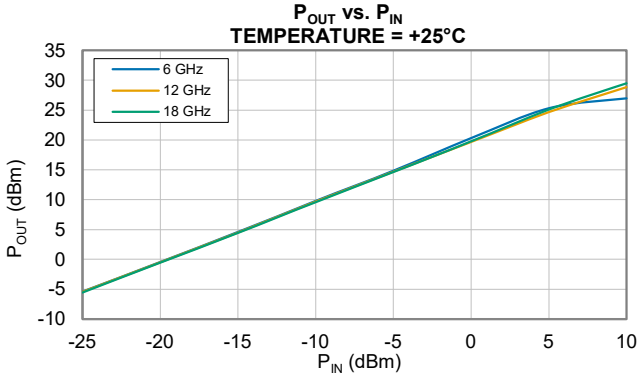
GAIN vs. P_{IN}
TEMPERATURE = +25°C



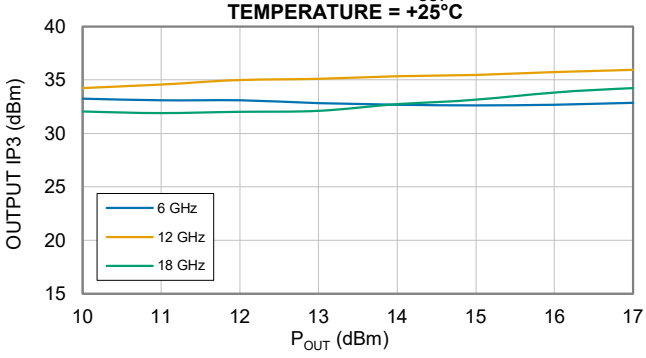
I_{DD} vs. P_{IN}
TEMPERATURE = +25°C



P_{OUT} vs. P_{IN}
TEMPERATURE = +25°C



OUTPUT IP3 vs. P_{OUT}
TEMPERATURE = +25°C



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ABSOLUTE MAXIMUM RATINGS[12]

Parameter	Ratings
Operating Temperature[13]	-55°C to +85°C
Storage Temperature[14]	-65°C to +150°C
Total Power Dissipation	6.5 W
Junction Temperature[15]	+175°C
Input Power (CW), V_{DD}[16] = +6 V	+26 dBm
DC Voltage on RF-OUT	+10 V
DC Voltage on RF-IN	+10 V
DC Drain Voltage on V_{DD}	+7.5 V
DC Drain Current I_{DD}[17]	1400 mA
DC Gate Voltage on V_{GG}[18]	-3 V < V_{GG} < 0 V
DC Gate Current I_{GG}[19]	5 mA

12. Permanent damage may occur if any of these limits are exceeded. Maximum ratings are not intended for continuous normal operation.
13. Bottom of die.
14. For die shipped in Gel-Pak see ENV-80 (limited by packaging).
15. Peak temperature on top of die.
16. $V_{DD} = V_{D1} = V_{D2}$
17. I_{DD} is the sum of the current of the I_{D1} and I_{D2} pads.
18. $V_{GG} = V_G$
19. I_{GG} is the sum of the current of the I_G pads.

THERMAL RESISTANCE

Parameter	Ratings
Thermal Resistance (Θ_{JC})[20]	18.3°C/W

20. Θ_{JC} = (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

ESD RATING[21]

	Class	Voltage Range	Reference Standard
HBM	1A	250 V < 500 V	ANSI/ESDA/JEDEC JS-001-2023
CDM	C3	> 1000 V	ANSI/ESDA/JEDEC JS-002-2022

21. ESD measured in 5 x 5 mm 32-Lead QFN-style package.

ESD HANDLING PRECAUTION: This device is designed to be Class 1A for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage.

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FUNCTIONAL DIAGRAM

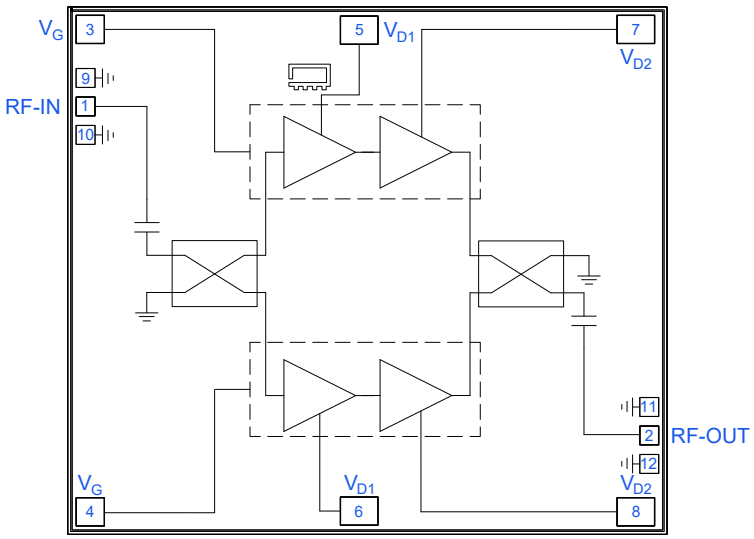

Figure 1. AVA-6183MP-D+ Functional Diagram

PAD DESCRIPTION

Function	Pad Number	Description (Refer to Figure 3)
RF-IN	1	RF-IN pad connects to RF-Input port.
RF-OUT	2	RF-OUT pad connects to RF-Output port.
V_{D1}	5, 6	DC Input pads connects to voltage input ports, V_{D1}.
V_{D2}	7, 8	DC Input pads connects to voltage input ports, V_{D2}.
V_G	3, 4	DC Input pads connect to voltage input ports, V_G.
GND	9-12, & Bottom of Die	Connected to die backside through vias. Bond wires to ground are optional.

DIE OUTLINE: INCHES [mm], TYPICAL

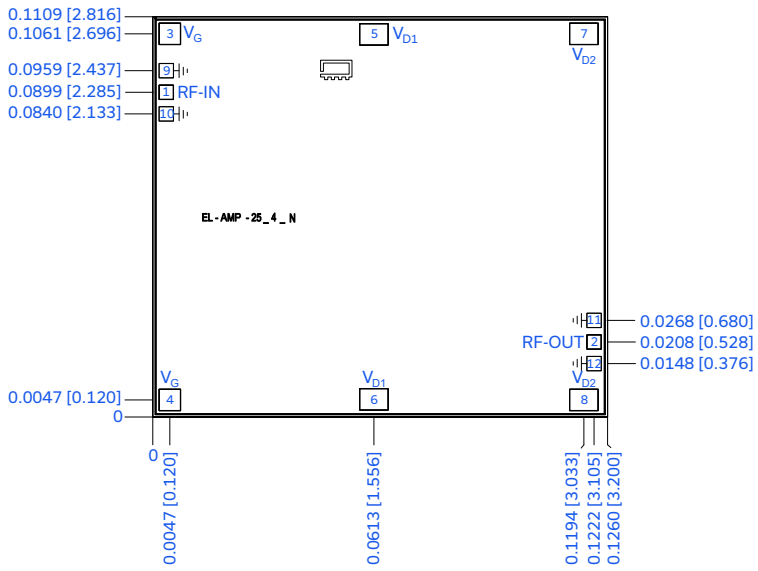

Figure 2. AVA-6183MP-D+ Die Outline

DIMENSIONS: INCHES [mm], TYPICAL

Die Size	0.1259 x 0.1108 [3.200 x 2.816]
Die Thickness	0.0040 [0.100]
Bond Pad Size	
Pad 1-2, 9-12	0.0040 x 0.0040 [0.102 x 0.102]
Pad 3-4	0.0060 x 0.0060 [0.152 x 0.152]
Pad 5-8	0.0080 x 0.0060 [0.202 x 0.152]
Plating (Pads & Bottom of Die)	Gold

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CHARACTERIZATION BOARD

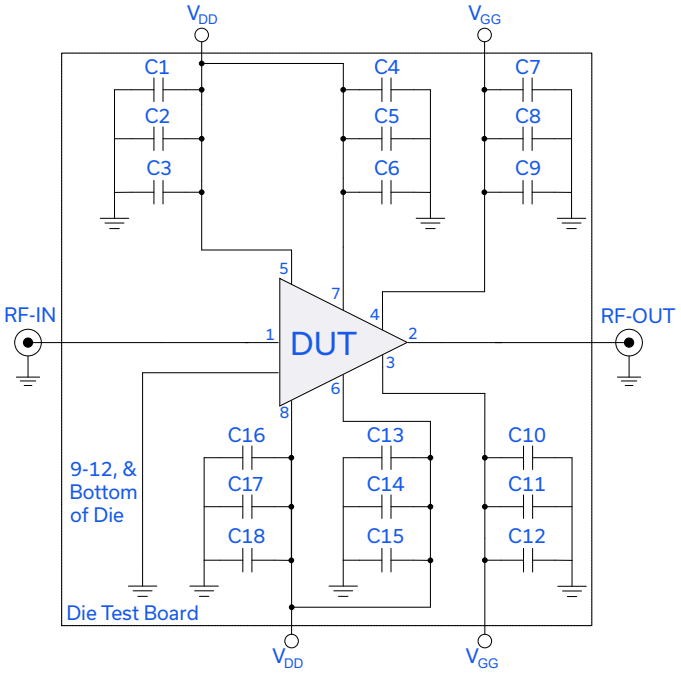

Figure 3. AVA-6183MP-D+ Characterization and Application Circuit

Electrical Parameters and Conditions
Gain, Return Loss, Output Power at 1 dB Compression (P1dB), Output Power at Saturation (P_{SAT}), Output IP3 (OIP3), and Noise Figure measured using N52425A PNA-X Microwave Network Analyzer.

Conditions:
1. Gain and Return Loss: P_{IN} = -25 dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, +16 dBm/tone at output

Power ON/Power OFF Sequence:
Caution: Permanent damage to the device will occur if the Power ON and Power OFF sequences are not followed.

Power ON:
1) Set V_{GG} = -2 V. Apply V_{GG}.
2) Set V_{DD} = +6 V. Apply V_{DD}.
3) Increase V_{GG} to obtain the desired I_{DD} as shown in specification table.
4) Apply RF Signal.

Power OFF:
1) Turn off RF Signal.
2) Adjust V_{GG} to -2 V.
3) Turn off V_{DD}.
4) Turn off V_{GG}.

Component	Value	Size	Part Number	Manufacturer
C3, C6, C9, C10, C13, C16	100 pF	0.022 x 0.022 in	MA4M3100	MACOM
C2, C5, C8, C11, C14, C17	0.01 µF	0402	04025C103KAT2A	AVX
C1, C4, C7, C12, C15, C18	1 µF	0402	GRM155R61H105KE05D	Murata

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ASSEMBLY DIAGRAM

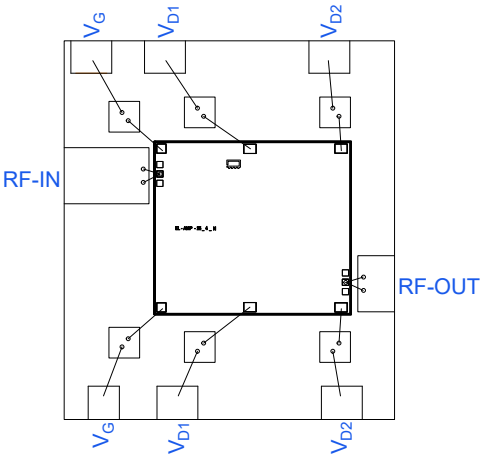

Figure 4. AVA-6183MP-D+ Assembly Diagram

- Bond wire diameter: 1 mil
- Bond wire lengths from die pad to PCB at RF-IN and RF-OUT: 11 mil ± 2 mils
- Bond wire length from die pads to capacitors near V_{D1}: 37 mil ± 2 mils
- Bond wire length from die pads to capacitors near V_{D2}: 22 mil ± 2 mils
- Bond wire length from die pads to capacitors near V_G: 29 mil ± 2 mils
- Typical gap from die edge to PCB edge: 3 mils
- PCB thickness and material: 8 mils RO4003C (Thickness: 1 oz copper on each side)

ASSEMBLY AND HANDLING PROCEDURE

1. Storage
   Die should be stored in a dry nitrogen purged desiccators or equivalent.
2. ESD
   MMIC pHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in anti-static protected material, which should be opened only in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
   Devices require careful handling using tools appropriate for manipulating semiconductor chips. It is recommended to handle the chips along the edges with a custom designed collet. The surface of the chips have exposed air bridges and should not be touched with a vacuum collet, tweezers or fingers.
   The die mounting surface must be clean and flat. Using conductive silver-filled epoxy, apply sufficient adhesive to meet the required bond line thickness, fillet height and coverage around the total periphery of the device. The recommended epoxy is Atrox 800HT5 or equivalent. Parts should be cured in a nitrogen-filled atmosphere per manufacturer's recommended cure profile.
4. Wire Bonding
   Openings in the surface passivation above the gold bond pads are provided to allow wire bonding to the die. Thermosonic bonding is recommended with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. The suggested interconnect is pure gold, 1 mil diameter wire. Bonds are recommended to be made from the bond pads on the die to the package or substrate. All bond wire length and bond wire height should be kept as short as possible, unless specified by design, to minimize performance degradation due to undesirable series inductance.

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ADDITIONAL DETAILED TECHNICAL INFORMATION IS AVAILABLE ON OUR DASHBOARD. CLICK HERE

Performance Data & Graphs	Data Graphs S-Parameter (S2P Files) Data Set (.zip file)
Case Style	Die
RoHS Status	Compliant
Die Ordering and Packaging Information	Quantity, Package — Model No. Gel - Pak: 5,10,50 KGD* — AVA-6183MP-DG+ Medium†, Partial wafer: KGD*<288 — AVA-6183MP-DP+ Full wafer† — AVA-6183MP-DF+ †Available upon request contact sales representative. Refer to AN-60-067
Die Marking	EL-AMP-25_4_N
Environmental Ratings	ENV80

*Known Good Die ("KGD") means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within a predefined range. While DC testing is not definitive, it does provide a high degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

NOTES

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuits' applicable established test performance criteria and measurement instructions.

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