MMIC DIE

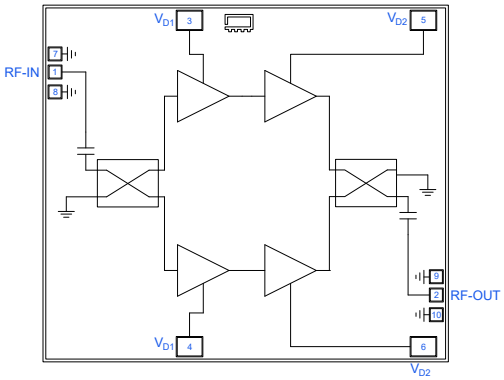
Medium Power Amplifier AVA-6183MPS-D+

50Ω 6 to 18 GHz Self Biased

THE BIG DEAL

- High Saturated Output Power, Typ. +28.4 dBm
- High Gain, Typ. 20.9 dB
- Single Supply Voltage +6 V at 663 mA

FUNCTIONAL DIAGRAM



SEE ORDERING INFORMATION ON THE LAST PAGE

APPLICATIONS

- 5G MIMO and Backhaul Radio
- Radar, EW, and ECM Defense Systems
- Satellite Communication
- Test and Measurement Equipment

PRODUCT OVERVIEW

Mini-Circuits' AVA-6183MPS-D+ is a wideband, medium power MMIC amplifier fabricated on a GaAs pHEMT process with high output power and broadband gain. Operating from 6 to 18 GHz, this amplifier features typical +26.9 dBm P1dB, +28.4 dBm P_{SAT}, and 20.9 dB gain while operating from a single +6 V power supply. The AVA-6183MPS-D+ is a two-stage, balanced amplifier that is internally matched to 50Ω and that measures only 2.81x3.2 mm. These characteristics make it the ideal driver amplifier for a wide range of applications including backhaul radio, radar and satellite communications.

KEY FEATURES

Feature	Advantages
Self Biased	Simplifies circuit design by eliminating the need for external biasing components, reducing PCB footprint and lowering the cost of integration.
High Gain, Typ. 20.9 dB	The MMIC amplifier's high gain enables fewer system components in receiver signal chains.
High Saturated Output Power, Typ. +28.4 dBm	High saturated output power and high gain make this amplifier ideal as a driver amplifier in 5G MIMO, backhaul radio, satellite communication, and EW applications.
Unpackaged Die	Suitable for chip and wire hybrid assemblies.

REV. OR
ECO-025280
AVA-6183MPS-D+
MCL NY
250421

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ELECTRICAL SPECIFICATIONS[1] AT +25°C, V_{DD} = +6 V, AND Zo = 50Ω UNLESS NOTED OTHERWISE

Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency Range		6		18	GHz
Gain	6		21.7		dB
	9		21.4		
	12		20.9		
	15		20.6		
	18		23.2		
Input Return Loss	6		16		dB
	9		17		
	12		14		
	15		20		
	18		18		
Output Return Loss	6		18		dB
	9		16		
	12		19		
	15		20		
	18		20		
Isolation	6-18		57.2		dB
Output Power at 1 dB Compression (P1dB)	6		+25.7		dBm
	9		+27.6		
	12		+26.9		
	15		+27.1		
	18		+27.5		
Output Power at Saturation (P_{SAT})[2]	6		+28.3		dBm
	9		+29.2		
	12		+28.4		
	15		+28.4		
	18		+28.6		
Output Third-Order Intercept (OIP3) (P_{OUT} = +12 dBm/Tone)	6		+33.9		dBm
	9		+33.4		
	12		+33.3		
	15		+33.2		
	18		+32.2		
Noise Figure	6		9.4		dB
	9		6.8		
	12		5.8		
	15		5.3		
	18		5.5		
Device Operating Voltage (V_{DD})[3,4]		+5	+6	+7	V
Device Operating Current (I_{DD})[5,6]			663		mA
Device Current Variation vs. Temperature[7]			-0.325		mA/°C
Device Current Variation vs. Voltage[8]			+10.3		µA/mV

1. Tested on Mini-Circuits Die Characterization Test Board. See Figure 3. Loss de-embedded to the RF input and output wire bonds of the device.
2. Defined as output power at which change is 0.1 dB per 1 dB change in input power
3. $V_{DD} = V_{D1} = V_{D2}$
4. Voltage must be applied to all V_{D1} and V_{D2} pins for standard operation.
5. Current at P_{IN} = -25 dBm. Increases to 810 mA at P_{SAT}.
6. $I_{DD} = I_{D1} + I_{D2}$
7. (Current at +85°C - Current at -55°C)/(+85°C - -55°C)
8. (Current at +7 V - Current at +5 V)/(+7 V - +5 V)

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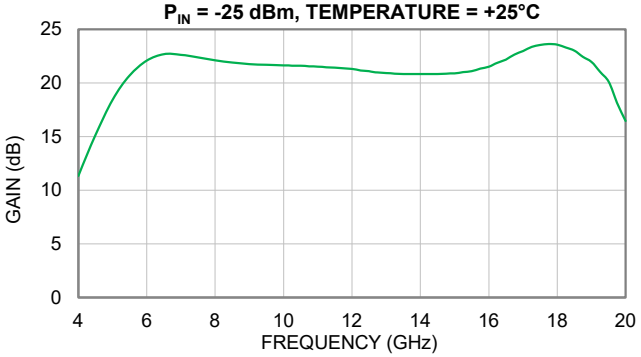
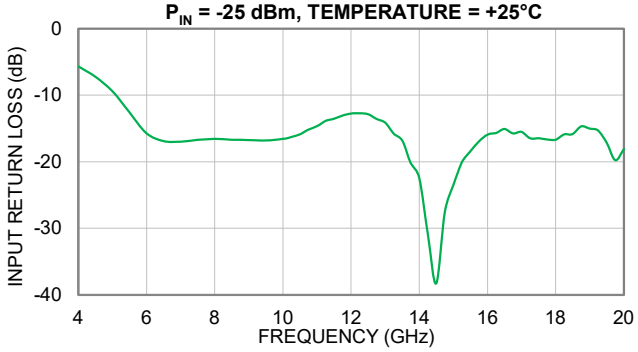
TYPICAL PERFORMANCE GRAPHS

Note: All data taken at V_{DD} = +6 V. For over voltage and temperature data, see AVA-6183MPS+.

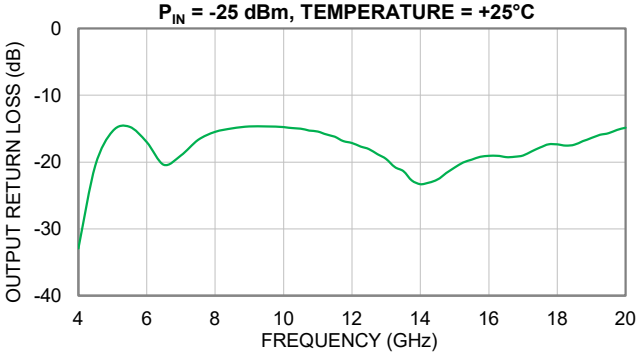
GAIN vs. FREQUENCY
P_{IN} = -25 dBm, TEMPERATURE = +25°C



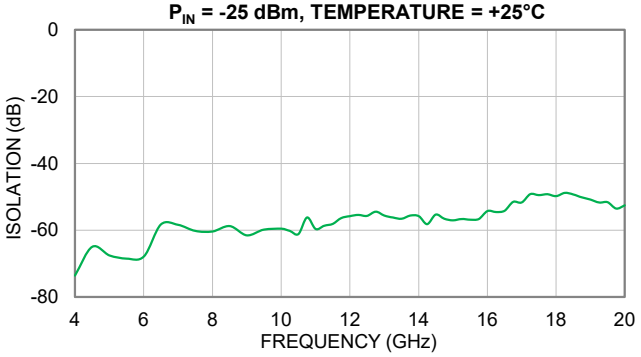
INPUT RETURN LOSS vs. FREQUENCY
P_{IN} = -25 dBm, TEMPERATURE = +25°C



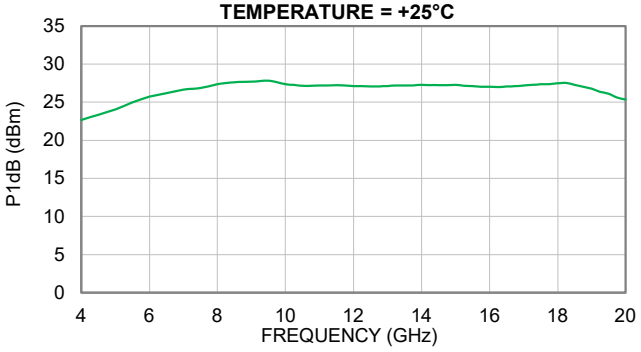
OUTPUT RETURN LOSS vs. FREQUENCY
P_{IN} = -25 dBm, TEMPERATURE = +25°C



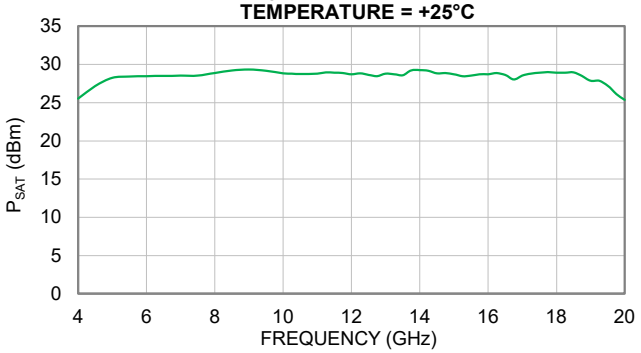
ISOLATION vs. FREQUENCY
P_{IN} = -25 dBm, TEMPERATURE = +25°C



P1dB vs. FREQUENCY
TEMPERATURE = +25°C



P_{SAT} vs. FREQUENCY
TEMPERATURE = +25°C



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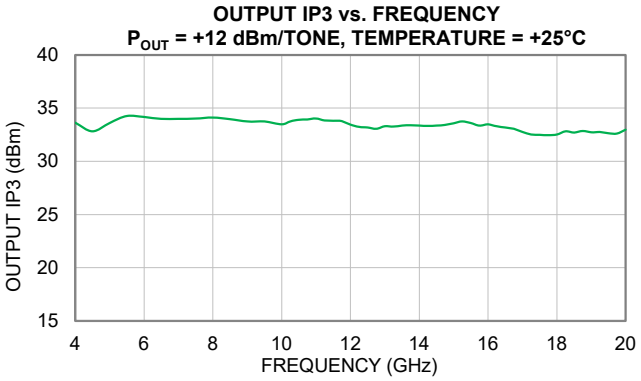
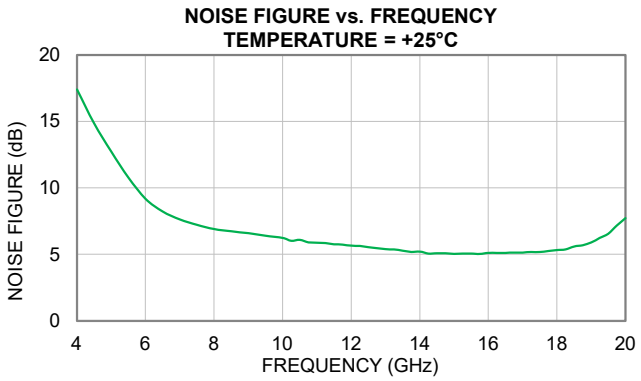
50Ω 6 to 18 GHz Self Biased

TYPICAL PERFORMANCE GRAPHS

Note: All data taken at V_{DD} = +6 V. For over voltage and temperature data, see AVA-6183MPS+.





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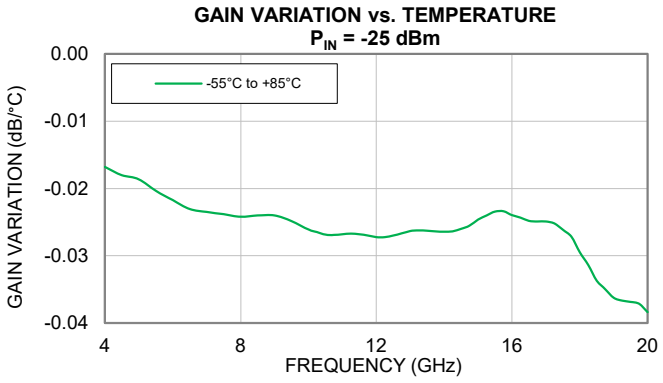
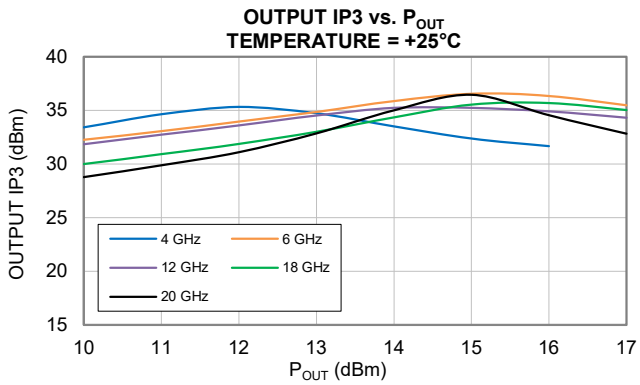
50Ω 6 to 18 GHz Self Biased

TYPICAL PERFORMANCE GRAPHS

Note: All data taken in this section represents the die attached in a 5x5 mm 32-Lead QFN-style package and measured on Mini-Circuits Characterization Test Board TB-AVA6183MPSC+. Data was taken at V_{DD} = +6 V.





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ABSOLUTE MAXIMUM RATINGS[9]

Parameter	Ratings
Operating Temperature[10]	-55°C to +85°C
Storage Temperature[11]	-65°C to +150°C
Total Power Dissipation	4.8 W
Junction Temperature[12]	+175°C
Input Power (CW), V_{DD}[13] = +6 V	+26 dBm
DC Voltage on RF-OUT	+10 V
DC Voltage on RF-IN	+10 V
DC Drain Voltage on V_{DD}	+10 V
DC Drain Current I_{DD}[14]	900 mA

9. Permanent damage may occur if any of these limits are exceeded. Maximum ratings are not intended for continuous normal operation.
10. Bottom of die.
11. For die shipped in Gel-Pak see ENV-80 (limited by packaging).
12. Hot spot temperature on top of die.
13. $V_{DD} = V_{D1} = V_{D2}$
14. $I_{DD} = I_{D1} = I_{D2}$

THERMAL RESISTANCE

Parameter	Ratings
Thermal Resistance (Θ_{JC})[15]	18.6 °C/W

15. Θ_{JC} = (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

ESD RATING[16]

	Class	Voltage Range	Reference Standard
HBM	1A	250 V < 500 V	ANSI/ESDA/JEDEC JS-001-2023
CDM	C3	> 1000 V	ANSI/ESDA/JEDEC JS-002-2022

16. ESD measured in 5 x 5 mm 32-Lead QFN-style package.

ESD HANDLING PRECAUTION: This device is designed to be Class 1A for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage.

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FUNCTIONAL DIAGRAM

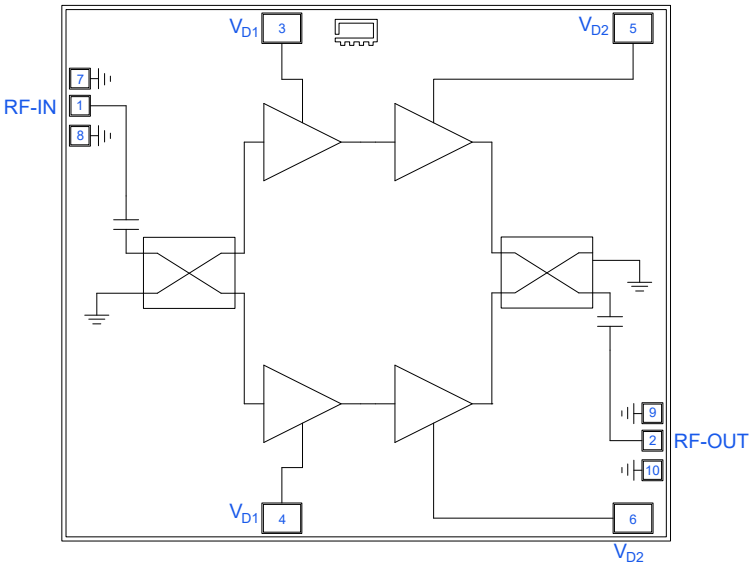

Figure 1. AVA-6183MPS-D+ Functional Diagram

PAD DESCRIPTION

Function	Pad Number	Description (Refer to Figure 3)
RF-IN	1	RF-IN pad connects to RF-Input port.
RF-OUT	2	RF-OUT pad connects to RF-Output port.
V_{D1}	3,4	DC Input pads connects to voltage input ports, V_{D1}.
V_{D2}	5,6	DC Input pads connects to voltage input ports, V_{D2}.
GND	7-10, & Bottom of Die	Connected to die backside through vias. Bond wires to ground are optional.

DIE OUTLINE: INCHES [mm], TYPICAL

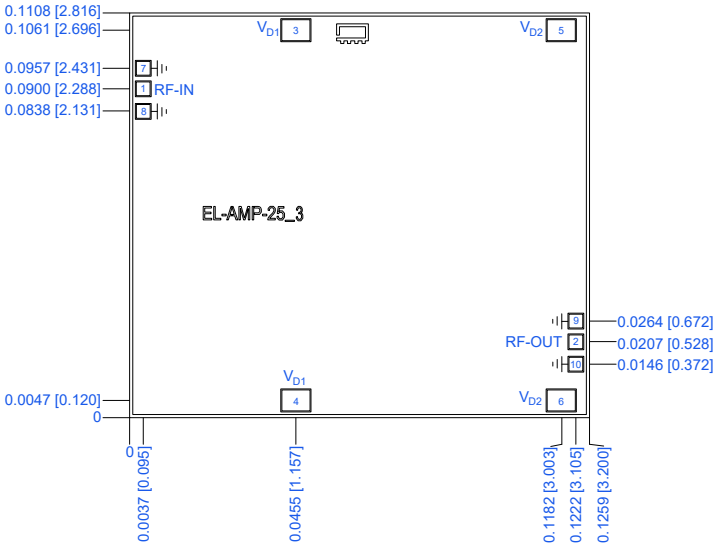

Figure 2. AVA-6183MPS-D+ Die Outline

DIMENSIONS: INCHES [mm], TYPICAL

Die Size	0.1259 x 0.1108 [3.200 x 2.816]
Die Thickness	0.0040 [0.100]
Bond Pad Size	
Pad 1-2, 7-10	0.0037 x 0.0037 [0.096 x 0.096]
Pad 3-6	0.0077 x 0.0057 [0.196 x 0.146]
Plating (Pads & Bottom of Die)	Gold

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CHARACTERIZATION BOARD

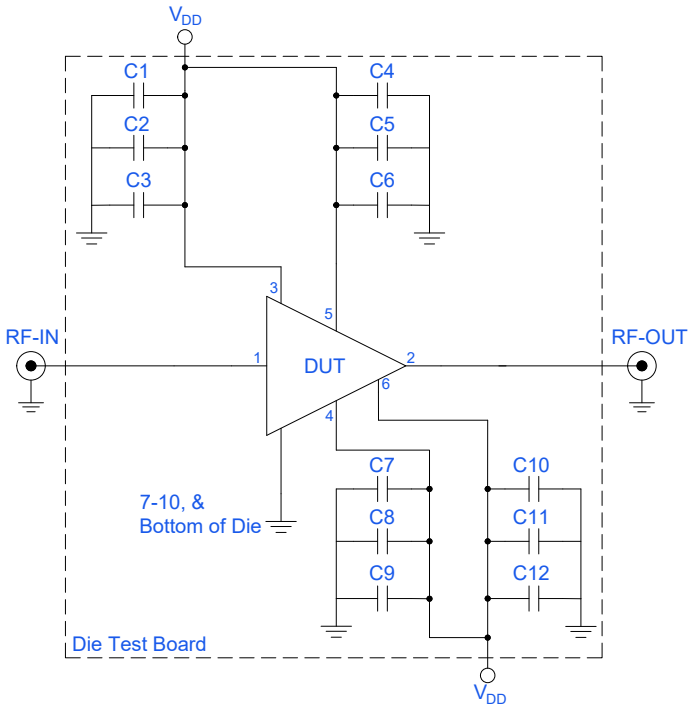

Figure 3. AVA-6183MPS-D+ Characterization and Application Circuit

Electrical Parameters and Conditions
Gain, Return Loss, Output Power at 1 dB Compression (P1dB), Output Power at Saturation (P_{SAT}), Output IP3 (OIP3), and Noise Figure measured using N52425A PNA-X Microwave Network Analyzer.

Conditions:
1. Gain and Return Loss: P_{IN} = -25 dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, +12 dBm/tone at output.

Power ON/Power OFF Sequence:
AVA-6183MPS-D+ is not sensitive to power ON/OFF sequence. V_{D1} and V_{D2} can be applied in any order. All voltage lines may be tied together and applied simultaneously.

Component	Value	Size	Part Number	Manufacturer
C3, C6, C7, C10	100 pF	0.022 x 0.022 in	MA4M3100	MACOM
C2, C5, C8, C11	0.01 µF	0402	04025C103KAT2A	AVX
C1, C4, C9, C12	1 µF	0402	GRM155R61H105KE05D	Murata

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ASSEMBLY DIAGRAM

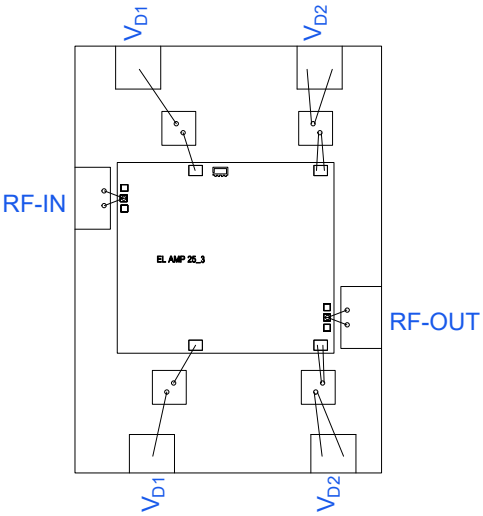

Figure 4. AVA-6183MPS-D+ Assembly Diagram

- Bond wire diameter: 1 mil
- Bond wire lengths from die pad to PCB at RF-IN & RF-OUT: 11 mil ± 2 mils
- Bond wire length from die pads to capacitors near V_{D1}: 66 mil ± 2 mils
- Bond wire length from die pads to capacitors near V_{D2}: 76 mil ± 2 mils
- Typical gap from die edge to PCB edge: 3 mils
- PCB thickness and material: 8 mils RO4003C (Thickness: 1 oz copper on each side)

ASSEMBLY AND HANDLING PROCEDURE

1. Storage
   Die should be stored in a dry nitrogen purged desiccators or equivalent.
2. ESD
   MMIC pHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in anti-static protected material, which should be opened only in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
   Devices require careful handling using tools appropriate for manipulating semiconductor chips. It is recommended to handle the chips along the edges with a custom designed collet. The surface of the chips have exposed air bridges and should not be touched with a vacuum collet, tweezers or fingers.
   The die mounting surface must be clean and flat. Using conductive silver-filled epoxy, apply sufficient adhesive to meet the required bond line thickness, fillet height and coverage around the total periphery of the device. The recommended epoxy is Atrox 800HT5 or equivalent. Parts should be cured in a nitrogen-filled atmosphere per manufacturer's recommended cure profile.
4. Wire Bonding
   Openings in the surface passivation above the gold bond pads are provided to allow wire bonding to the die. Thermosonic bonding is recommended with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. The suggested interconnect is pure gold, 1 mil diameter wire . Bonds are recommended to be made from the bond pads on the die to the package or substrate. All bond wire length and bond wire height should be kept as short as possible, unless specified by design, to minimize performance degradation due to undesirable series inductance.

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ADDITIONAL DETAILED TECHNICAL INFORMATION IS AVAILABLE ON OUR DASHBOARD. CLICK HERE

Performance Data & Graphs	Data Graphs S-Parameter (S2P Files) Data Set (.zip file)
Case Style	Die
RoHS Status	Compliant
Die Ordering and Packaging Information	Quantity, Package — Model No. Gel - Pak: 5,10,50 KGD* — AVA-6183MPS-DG+ Medium†, Partial wafer: KGD*<288 — AVA-6183MPS-DP+ Full wafer — AVA-6183MPS-DF+ †Available upon request contact sales representative. Refer to AN-60-067
Die Marking	EL-AMP-25_3
Environmental Ratings	ENV80

*Known Good Die ("KGD") means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within a predefined range. While DC testing is not definitive, it does provide a high degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

NOTES

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