

# Ceramic Balance Filter

50Ω 1710 to 2610 MHz

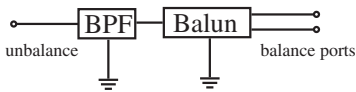
## Features

- Small size (0.126"x0.098"x0.039")
- Temperature stable
- Hermetically sealed

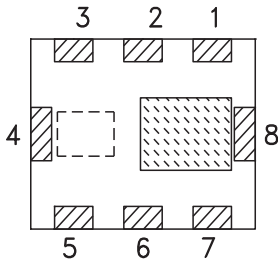
## Applications

- ISM
- Cellular

### Simplified Schematic



### Top View



### Pad Connections

Unbalanced Port	7
Balanced Port	3, 5
GND	2, 4, 8
GNC or DC Feed	6
NC	1

# BBFCV-2250+



Generic photo used for illustration purposes only

CASE STYLE: JV1210C-4

**+RoHS Compliant**

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Available Tape and Reel at no extra cost	
Reel Size	Devices/Reel
7"	20, 50, 100, 200, 500, 1000, 4000

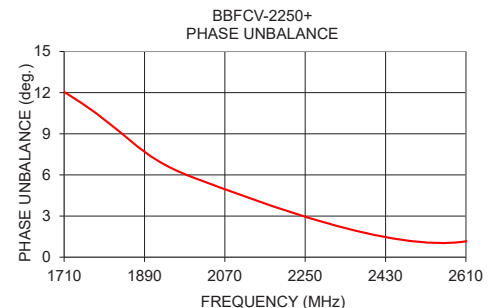
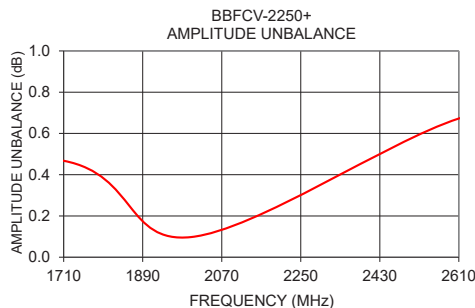
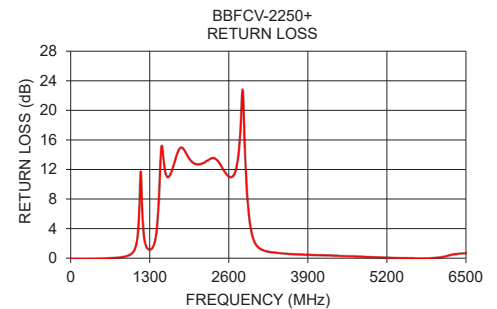
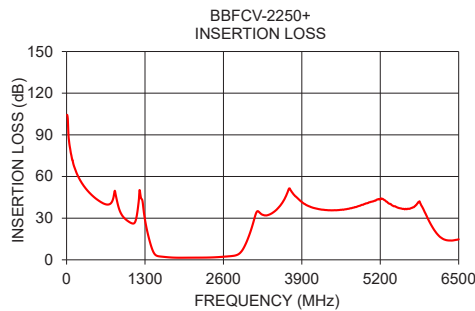
## Electrical Specifications at 25°C

Parameter	F#	Frequency (MHz)	Min.	Typ.	Max.	Unit
Impedance Ratio			2:1			
Insertion Loss	F1-F2	1710 - 2610	—	—	3.2	dB
Attenuation		10-670	35	—	—	dB
		670-1240	17	—	—	
		3390-5400	27	—	—	
		5400-6000	17	—	—	
Amplitude Unbalance		1710 - 2610	—	—	1.5	dB
Phase Unbalance		1710 - 2610	—	—	15	degree
Input VSWR		1710 - 2610	—	1.8	—	:1

### Maximum Ratings

Operating Temperature	-55°C to +105°C
Storage Temperature	-55°C to +105°C
RF Power Input*	1W @25°C

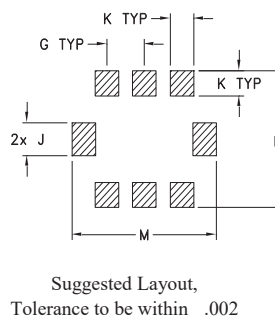
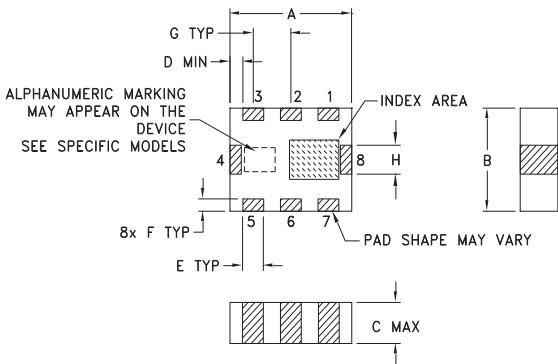
\* Refer to product storage temperature after installation  
Suggestion for T&R unused product storage condition: +5 ~ +35 °C,  
Humidity 45-75%RH, 12 month Max



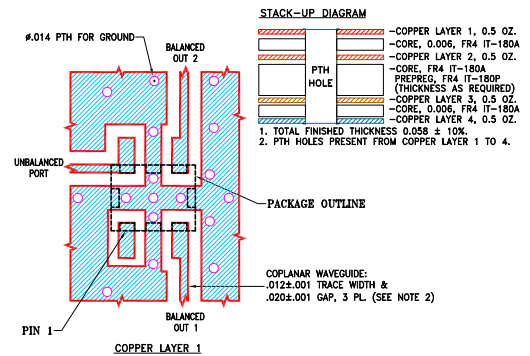
### Typical Performance Data

Frequency (MHz)	Insertion Loss (dB)	Return Loss (dB)	Amplitude Unbalance (dB)	Phase Unbalance (Deg.)
10	104.41	0.04	0.32	92.40
50	82.29	0.03	3.87	5.15
100	71.51	0.03	4.02	4.76
500	43.62	0.07	2.66	12.67
1000	28.43	0.75	0.50	25.45
1710	1.75	13.21	0.47	12.04
2000	1.54	13.03	0.10	5.80
2610	2.26	11.05	0.67	1.16
3000	14.60	2.64	0.79	10.88
3500	36.99	0.77	4.27	33.06
4000	38.92	0.55	0.48	14.44
4500	35.81	0.41	4.14	7.47
5000	40.97	0.26	3.86	58.46
5500	37.46	0.13	0.47	16.56
6000	28.71	0.20	0.12	33.44
6500	14.78	0.83	3.10	13.19

### Outline Drawing



### Demo Board MCL P/N: TB-1053+ Suggested PCB Layout (PL-632)



- NOTES:**
1. PCB IS MULTILAYER PCB, SEE STACK-UP DIAGRAM.
  2. TRACE WIDTH & GAP PARAMETERS ARE SHOWN FOR FR4 IT-180A WITH DIELECTRIC THICKNESS .006"±.0007"; COPPER: 1/2 OZ. FOR OTHER MATERIALS TRACE WIDTH AND GAP MAY NEED TO BE MODIFIED.
  3. LAYERS 2,3,4 OF THE PCB ARE CONTINUOUS GROUND PLANE.
- DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK

### Outline Dimensions (inch/mm)

A	B	C	D	E	F	G
.126	.098	.039	.004	.022	.012	.039
3.2	2.5	1.0	0.1	0.56	0.3	1.0
H	J	K	L	M	wt	
.028	.031	.024	.130	0.15	grams	
0.7	0.8	0.6	3.30	3.81	0.030	

### Additional Notes

- A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
- B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
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