Engineering Development Model

Frequency Synthesizer

DSN-EDR11167

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability.
At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.

Please click "Back", and then click "Contact Us" for Applications support.

CASE STYLE : 99-01-1928

ELECTRICAL SPECIFICATIONS 50Ω, over -30°C to +70°C					
Parameter		**Min.**	**Typ.**	**Max.**	**Units**
Frequency		1025		1475	MHz
Step size			100		kHz
Settling Time	**Within ±1kHz**		40		msec
Output Power		+10	+14	+18	dBm
Phase Noise					
	at 100 Hz offset		-89		dBc/Hz
	at 1 kHz offset		-97		dBc/Hz
	at 10 KHz offset		-98	-92	dBc/Hz
	at 100 KHz offset		-121	-115	dBc/Hz
	at 1000 kHz offset		-144		dBc/Hz
Integrated SSB Phase Noise			-52		dBc
Ref & Comp Spurious Suppression			-95		dBc
0.5 Step size Spurious Suppression			-107		dBc
Non-Harm. Spurious Suppression			-90		dBc
Harmonic Suppression			-44	-18	dBc
Supply voltage	**A-VCC**		5		V
	D-VCC		5		V
Supply current	**A-VCC**		68	78	V
	D-VCC		46	55	V
Reference In (External)	**Frequency**		10		MHz
	Amplitude		1		Vp-p
	Impedance		100		kΩ
	Ph. N @ 1kHz		-145		dBc/Hz
Input Logic Levels	**Logic high**	2		3.3	V
	Logic Low			0.5	
Digital Lock Detect	**Locked**	1.4		3.3	V
	Unlocked			0.4	
Frequency Synthesizer PLL		Automatic startup at specified frequency (via internal microcontroller) & user programable (ADF4153)			

ABSOLUTE MAXIMUM RATINGS	
Operating Temperature	-45°C to 85°C
Storage Temperature	-55°C to 100°C
A-VCC Supply Voltage	6V
D-VCC Supply Voltage	6V
Reference Frequency voltage	3.6Vp-p
Data, Clock & LE levels	3.6V

Power On sequence: A-VCC followed by D-VCC
Power Off sequence: D-VCC followed by A-VCC

PIN CONNECTIONS			
RF OUT	14	**CLOCK**	5
A-VCC	16	**DATA**	6
D-VCC	1	**LATCH ENABLE**	7
REF IN	8	**GROUND**	2,3,9,10,12,13,15
LOCK DETECT	4		