Engineering Development Model

Frequency Synthesizer

DSN-EDR8382

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



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CASE STYLE: LK942

ELECTRICAL SPECIFICATIONS 50Ω, over -45°C to +70°C						
Parameter		Min.	Тур.	Max.	Units	
Frequency		3040		3540	MHz	
Step size			125		kHz	
Settling Time W	/ithin ±1kHz		5		msec	
Output Power		-6	-2	+2	dBm	
Phase Noise						
	at 100 Hz offset		-79		dBc/Hz	
	at 1 kHz offset		-76	-70	dBc/Hz	
	at 10 KHz offset		-87	-81	dBc/Hz	
	at 100 KHz offset		-117		dBc/Hz	
	at 1000 kHz offset		-137	-131	dBc/Hz	
Integrated SSB Phase Noise			-37		dBc	
Comparison Spurious Suppression			-86		dBc	
0.5 Step size Spurious Suppression			-106		dBc	
Non-Harm. Spurious Suppression			-90		dBc	
Harmonic Suppression			-28		dBc	
Supply voltage	VCO		5		V	
Supply voltage	PLL		15		V	
Supply current	VCO		48	57	mA	
	PLL		14	22	mA	
	Frequency		81		MHz	
Reference In	Amplitude		1		Vp-p	
(External)	Impedance		100		kΩ	
	Ph. N @ 1kHz		-145		dBc/Hz	
Input Logic	Logic high	1.4		3.3	V	
Levels	Logic Low			0.6	V	
Digital Lock	Locked	1.4		3.3	V	
Detect	Unlocked			0.4	<u> </u>	
Frequency Synthesizer PLL			ADF41	53		

ABSOLUTE MAXIMUM RATINGS				
Operating Temperature	-50°C to 85°C			
Storage Temperature	-55°C to 100°C			
VCO Supply Voltage	6V			
PLL Supply Voltage	16V			
Reference Frequency voltage	3.6Vp-p			
Data, Clock & LE levels	3.6V			

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS					
RF OUT	5	CLOCK	11		
VCC VCO	16	DATA	9		
VCC PLL	18	LATCH ENABLE	12		
REF IN	14	GROUND	2,4,6,8,13,14		
LOCK DETECT	7				