Engineering Development Model

Frequency Synthesizer DSN-EDR9496/3MP

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability.
At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.

Please click "Back", and then click "Contact Us" for Applications support.

CASE STYLE : KL942

ELECTRICAL SPECIFICATIONS 50Ω, over -29°C to +60°C					
Parameter		**Min.**	**Typ.**	**Max.**	**Units**
Frequency		56.25		99.9938	MHz
Step size			6.25		kHz
Settling Time	Within ±1kHz		150		msec
Output Power		-7	+5	+10	dBm
Phase Noise					
	at 100 Hz offset		-41		dBc/Hz
	at 1 kHz offset		-66		dBc/Hz
	at 10 KHz offset		-85		dBc/Hz
	at 100 KHz offset		-102		dBc/Hz
	at 1000 kHz offset		-118		dBc/Hz
Integrated SSB Phase Noise			-37		dBc
Reference Spurious Suppression			-69		dBc
Comparison Spurious Suppression			-99		dBc
Non-Harm. Spurious Suppression			-90		dBc
Harmonic Suppression			-40		dBc
Supply voltage	VCO		5		V
	PLL		17		V
Supply current	VCO		10	32	V
	PLL		6	21	V
Reference In (External)	Frequency		52		MHz
	Amplitude		1		Vp-p
	Impedance		100		kΩ
	Ph. N @ 1kHz		-145		dBc/Hz
Input Logic Levels	Logic high	2.64		3.3	V
	Logic Low			0.66	
Digital Lock Detect	Locked	2.9		3.3	V
	Unlocked			0.4	
Frequency Synthesizer PLL		LMX2306			

ABSOLUTE MAXIMUM RATINGS	
Operating Temperature	-45°C to 85°C
Storage Temperature	-55°C to 100°C
VCO Supply Voltage	6V
PLL Supply Voltage	18V
Reference Frequency voltage	5.8Vp-p
Data, Clock & LE levels	3.6V

Power On sequence: Vcc VCO followed by Vcc PLL
Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS			
RF OUT	5	**CLOCK**	11
VCC VCO	16	**DATA**	9
VCC PLL	18	**LATCH ENABLE**	7
REF IN	14	**GROUND**	1,2,3,4,6,8,10,13,15, 17,19,20,21,22
LOCK DETECT	7		