Engineering Development Model

Frequency Synthesizer

DSN-EDR9520

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



Please click "Back", and then click "Contact Us" for Applications support.

CASE	STYLE :	KL942
U, 10_	•	

ELECTRICAL SPECIFICATIONS 50Ω, over -45°C to +85°C						
Parameter		Min.	Тур.	Max.	Units	
Frequency		870		1300	MHz	
Step size			5000		kHz	
Settling Time Within	±1kHz		12		μsec	
Output Power		-3	+1	+5	dBm	
	at 100 Hz offset at 1 kHz offset at 10 KHz offset at 100 KHz offset		-93 -103 -104 -103	-97 -98 -97	dBc/Hz dBc/Hz dBc/Hz dBc/Hz	
	at 1000 kHz offset		-125	.07	dBc/Hz	
Integrated SSB Phase Noise			-47		dBc	
Comparison Spurious Suppression		- O	-94		dBc	
Non-Harm. Spurious Suppre	ession		-90		dBc	
Harmonic Suppression			-32		dBc	
Supply voltage	VCO PLL		5		V V	
Supply current	VCO PLL		42 10	50 18	mA mA	
Reference In (External)	Frequency Amplitude Impedance h. N @ 1kHz		50 1 100 -145		MHz Vp-p kΩ dBc/Hz	
Levels	Logic high Logic Low	1,4		3.2 0.6 3.2	V	
	Locked Unlocked	2.8	.==	0.4	V	
Frequency Synthesizer PLL		ADF4106				

ABSOLUTE MAXIMUM RATINGS					
Operating Temperature	-45°C to 85°C				
Storage Temperature	-55°C to 100°C				
VCO Supply Voltage	6V				
PLL Supply Voltage	6V				
Reference Frequency voltage	3.6Vp-p				
Data, Clock & LE levels	3.5V				

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS						
RF OUT	5	CLOCK	14			
VCC VCO	16	DATA	16			
VCC PLL	18	LATCH ENABLE	18			
REF IN	14	GROUND	1-4,6,8,10,13,			
LOCK DETECT	7	GROUND	15,17,19-22			