Engineering Development Model

Frequency Synthesizer KSN-EDR101771MP

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability.
At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.

Please click "Back", and then click "Contact Us" for Applications support.

CASE STYLE : DK1042

ELECTRICAL SPECIFICATIONS 50Ω, over -45°C to +75°C					
Parameter		**Min.**	**Typ.**	**Max.**	**Units**
Frequency		930		1470	MHz
Step size			5000		kHz
Settling Time	**Within ±1kHz**		70		µsec
Output Power		-1	+3	+7	dBm
Phase Noise					
	at 100 Hz offset		-89		dBc/Hz
	at 1 kHz offset		-97		dBc/Hz
	at 10 KHz offset		-98		dBc/Hz
	at 100 KHz offset		-98		dBc/Hz
	at 1000 kHz offset		-127		dBc/Hz
Integrated SSB Phase Noise			-45		dBc
Reference Spurious Suppression			-90		dBc
Comparison Spurious Suppression			-93		dBc
Non-Harm. Spurious Suppression			-90		dBc
Harmonic Suppression			-19		dBc
Supply voltage	**VCO**		3.3		V
	PLL		3.3		V
Supply current	**VCO**		31	40	V
	PLL		8	17	V
Reference In (External)	**Frequency**		10		MHz
	Amplitude		1		Vp-p
	Impedance		100		kΩ
	Ph. N @ 1kHz		-145		dBc/Hz
Input Logic Levels	**Logic high**	2.64		3.3	V
	Logic Low			0.66	
Digital Lock Detect	**Locked**	2.9		3.3	V
	Unlocked			0.4	
Frequency Synthesizer PLL		ADF4112			

ABSOLUTE MAXIMUM RATINGS	
Operating Temperature	-45°C to 85°C
Storage Temperature	-55°C to 100°C
VCO Supply Voltage	4.3V
PLL Supply Voltage	4.3V
Reference Frequency voltage	5.8Vp-p
Data, Clock & LE levels	3.6V

Power On sequence: Vcc VCO followed by Vcc PLL
Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS			
RF OUT	7	**CLOCK**	10
VCC VCO	5	**DATA**	11
VCC PLL	1	**LATCH ENABLE**	12
REF IN	3	**GROUND**	2,4,6,8,13,14
LOCK DETECT	9		