*Engineering Development Model*

# Frequency Synthesizer KSN-EDR10427

### Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability.
At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.

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**CASE STYLE : DK1042**



| ELECTRICAL SPECIFICATIONS 50Ω, over -40°C to +85°C | | | | | |
|---|---|---|---|---|---|
| **Parameter** | | **Min.** | **Typ.** | **Max.** | **Units** |
| **Frequency** | | 1930 | | 2020 | MHz |
| **Step size** | | | 100 | | kHz |
| **Settling Time** | Within ±1kHz | | 2 | | msec |
| **Output Power** | | -2 | +2 | +6 | dBm |
| **Phase Noise** | | | | | |
| | at 100 Hz offset | | -75 | | dBc/Hz |
| | at 1 kHz offset | | -73 | -67 | dBc/Hz |
| | at 10 KHz offset | | -88 | -82 | dBc/Hz |
| | at 100 KHz offset | | -122 | | dBc/Hz |
| | at 1000 kHz offset | | -147 | -142 | dBc/Hz |
| **Integrated SSB Phase Noise** | | | -62 | | dBc |
| **Reference Spurious Suppression** | | | -102 | | dBc |
| **Comparison Spurious Suppression** | | | -115 | | dBc |
| **Non-Harm. Spurious Suppression** | | | -90 | | dBc |
| **Harmonic Suppression** | | | -52 | | dBc |
| **Supply voltage** | VCO | | 5 | | V |
| | PLL | | 5 | | V |
| **Supply current** | VCO | | 31 | 39 | V |
| | PLL | | 8 | 17 | V |
| **Reference In (External)** | Frequency | | 10 | | MHz |
| | Amplitude | | 1 | | Vp-p |
| | Impedance | | 100 | | kΩ |
| | Ph. N @ 1kHz | | -145 | | dBc/Hz |
| **Input Logic Levels** | Logic high | 4 | | 5 | V |
| | Logic Low | | | 1 | |
| **Digital Lock Detect** | Locked | 4.6 | | 5 | V |
| | Unlocked | | | 0.4 | |
| **Frequency Synthesizer PLL** | | | ADF4118 | | |

| ABSOLUTE MAXIMUM RATINGS | |
|---|---|
| **Operating Temperature** | -45°C to 85°C |
| **Storage Temperature** | -55°C to 100°C |
| **VCO Supply Voltage** | 6V |
| **PLL Supply Voltage** | 6V |
| **Reference Frequency voltage** | 5.8Vp-p |
| **Data, Clock & LE levels** | 5.3V |

Power On sequence: Vcc VCO followed by Vcc PLL
Power Off sequence: Vcc PLL followed by Vcc VCO

| PIN CONNECTIONS | | | |
|---|---|---|---|
| **RF OUT** | 7 | **CLOCK** | 10 |
| **VCC VCO** | 5 | **DATA** | 11 |
| **VCC PLL** | 1 | **LATCH ENABLE** | 12 |
| **REF IN** | 3 | **GROUND** | 2,4,6,8,13,14 |
| **LOCK DETECT** | 9 | | |