Engineering Development Model

Frequency Synthesizer

KSN-EDR108021SA

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



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CASE STYLE: DK1042

| ELECTRICAL SPECIFICATIONS 50Ω, over -15°C to +75°C | | | | | | |
|--|--|--------------------------|------------------------|----------------------|-----------------------------|--|
| Parameter | | Min | Тур. | Max. | Units | |
| Frequency | | 850 | | 850 | MHz | |
| Step size | | | 10000 | | kHz | |
| Settling Time Wit | thin ±1kHz | | 200 | | usec | |
| Output Power | | -1 | +3 | +6 | dBm | |
| Phase Noise | at 100 Hz offset | | -99 111 | -105 | dBc/Hz dBc/Hz | |
| | at 10 KHz offset at 100 KHz offset | | -110 -125 | -105 -105 -119 | dBc/Hz dBc/Hz | |
| | at 1000 kHz offset | | -156 | -150 | dBc/Hz | |
| Integrated SSB Phase Noise | | | -62 | | dBc | |
| Ref & Comp Spurious Suppression | | | -87 | | dBc | |
| Non-Harm. Spurious Suppression | | | -90 | | dBc | |
| Harmonic Suppression | | | -38 | -31 | dBc | |
| Supply voltage | VCO PLL | 26. | 5 3 | | V V | |
| Supply current | VCO PLL | | 42 | 50 17 | V V | |
| Reference In (External) | Frequency Amplitude Impedance Ph. N @ 1kHz | 70 | 10 1 100 -145 | | MHz Vp-p kΩ dBc/Hz | |
| Input Logic Levels | Logic high Logic Low | 1.4 | | 3 0.6 | V | |
| Digital Lock Detect | Locked Unlocked | 2.6 | | 3 0.4 | V | |
| Frequency Synthesizer PLL | | ADF4106 | | | | |
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| ABSOLUTE MAXIMUM RATINGS | | | | | |
|-----------------------------|----------------|--|--|--|--|
| Operating Temperature | -40°C to 85°C | | | | |
| Storage Temperature | -55°C to 100°C | | | | |
| VCO Supply Voltage | 6V | | | | |
| PLL Supply Voltage | 4V | | | | |
| Reference Frequency voltage | 3.6Vp-p | | | | |
| Data, Clock & LE levels | 3.3V | | | | |

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

| PIN CONNECTIONS | | | | | | |
|-----------------|---|--------------|---------------|--|--|--|
| RF OUT | 3 | CLOCK | 10 | | | |
| VCC VCO | 5 | DATA | 11 | | | |
| VCC PLL | 1 | LATCH ENABLE | 12 | | | |
| REF IN | 7 | GROUND | 2,4,6,8,13,14 | | | |
| LOCK DETECT | 9 | | | | | |

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.

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