## Engineering Development Model

## **Frequency Synthesizer**

## **KSN-EDR10966**

## **Important Note**

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



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**CASE STYLE: DK1042** 

ELECTRICAL SPECIFICATIONS 50Ω, over -55°C to +85°C						
Parameter	Min.	Тур.	Max.	Units		
Frequency	297.1		297.1	MHz		
Step size	•	100		kHz		
Settling Time Within ±1kHz	<b>A</b>	20		msec		
Output Power	-6	-2	+1	dBm		
Phase Noise						
at 100 Hz offset		-90		dBc/Hz		
at 1 kHz offset		-94	-88	dBc/Hz		
at 10 KHz offset		-109	-104	dBc/Hz		
at 100 KHz offset		-134	-128	dBc/Hz		
at 1000 kHz offset		152		dBc/Hz		
Integrated SSB Phase Noise		-56		dBc		
Reference Spurious Suppression		-100		dBc		
Comparison Spurious Suppression		-99		dBc		
Non-Harm. Spurious Suppression	<b>*</b> C	-90		dBc		
Harmonic Suppression		-33	-27	dBc		
Supply voltage VCO		5		V		
PLL PLL		5		V		
Supply current VC		36	44	V		
PLL PLL		11	19	V		
Frequency		100		MHz		
Reference In Amplitude		4		Vp-p		
(External) Impedance		100		kΩ		
Ph. N @ 1kHz	40	-145		dBc/Hz		
Input Logic Logic high	4		5	V		
Levels Logic Low	4 7 4		1	V		
Digital Lock Locked	4.6		5	V		
Detect Unlocked			0.4	V		

ABSOLUTE MAXIMUM RATINGS				
Operating Temperature	_55°C to 85°C			
Storage Temperature	-55°C to 100°C			
VCO Supply Voltage	6V			
PLLSupply Voltage	6V			
Reference Frequency voltage	5.8Vp-p			
Data, Clock & LE levels	5.3V			

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS					
RF OUT	7	N.C	10,11,12		
VCC VCO	5	GROUND	2,4,6,8,13,14		
VCC PLL	1				
REF IN	3				
LOCK DETECT	9				