Engineering Development Model

Frequency Synthesizer KSN-EDR10969

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability.
At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.

Please click "Back", and then click "Contact Us" for Applications support.

CASE STYLE : DK1042

ELECTRICAL SPECIFICATIONS 50Ω, over -40°C to +85°C					
Parameter		**Min.**	**Typ.**	**Max.**	**Units**
Frequency		2721.52		2737.52	MHz
Step size			80		kHz
Settling Time	**Within ±1kHz**		1.5		msec
Output Power		-2	+2	+6	dBm
Phase Noise					
	at 100 Hz offset		-83		dBc/Hz
	at 1 kHz offset		-90		dBc/Hz
	at 10 KHz offset		-97	-92	dBc/Hz
	at 100 KHz offset		-124	-118	dBc/Hz
	at 1000 kHz offset		-144	-138	dBc/Hz
Integrated SSB Phase Noise			-50		dBc
Reference Spurious Suppression			-109		dBc
Comparison Spurious Suppression			-95		dBc
Non-Harm. Spurious Suppression			-90		dBc
Harmonic Suppression			-28	-22	dBc
Supply voltage	**VCO**		5		V
	PLL		3		V
Supply current	**VCO**		46	52	V
	PLL		13	19	V
Reference In (External)	**Frequency**		10		MHz
	Amplitude		1		Vp-p
	Impedance		100		kΩ
	Ph. N @ 1kHz		-145		dBc/Hz
Input Logic Levels	**Logic high**	1.4		3	V
	Logic Low			0.6	
Digital Lock Detect	**Locked**	1.4		3	V
	Unlocked			0.4	
Frequency Synthesizer PLL		ADF4153			

ABSOLUTE MAXIMUM RATINGS	
Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 100°C
VCO Supply Voltage	6V
PLL Supply Voltage	4V
Reference Frequency voltage	3.6Vp-p
Data, Clock & LE levels	3.3V

Power On sequence: Vcc VCO followed by Vcc PLL
Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS			
RF OUT	7	**CLOCK**	10
VCC VCO	5	**DATA**	11
VCC PLL	1	**LATCH ENABLE**	12
REF IN	3	**GROUND**	2,4,6,8,13,14
LOCK DETECT	9		