Engineering Development Model

Frequency Synthesizer

KSN-EDR10978SA

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



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CASE STYLE: DK1171

ELECTRICAL SPECIFICATIONS 50Ω, over -40°C to +70°C						
Parameter	Min.	Тур.	Max.	Units		
Frequency	1625		1625	MHz		
Step size		15625		kHz		
Settling Time Within ±1kHz		0.25		msec		
Output Power	0	+3	+7	dBm		
Phase Noise at 100 Hz of at 1 kHz of		-91	00	dBc/Hz		
at 10 KHz of	fset	-98 -108	-92 -102	dBc/Hz dBc/Hz		
at 100 KHz of at 1000 kHz of		-118 -147	-112 -142	dBc/Hz dBc/Hz		
Integrated SSB Phase Noise		-57		dBc		
Reference Spurious Suppression		-101		dBc		
Comparison Spurious Suppression		-93		dBc		
Non-Harm. Spurious Suppression		-90		dBc		
Harmonic Suppression	40 '	-28	-21	dBc		
Supply voltage VCO PLL		5 3		V V		
Supply current PLL	4	29 12	37 20	V V		
Reference In (External) Frequency Amplitude Impedance Ph. N.@ 1kHz	S JOH	156,25 1 100 -145		MHz Vp-p kΩ dBc/Hz		
Input Logic Logic high Levels Logic Low	1.4	-145	3 0.6	V		
Digital Lock Detect Unlocked	2.6		3 0.4	V		
Frequency Synthesizer PLL ADF4106						

ABSOLUTE MAXIMUM RATINGS				
Operating Temperature	-45°C to 85°C			
Storage Temperature	-55°C to 100°C			
VCO Supply Voltage	6V			
PLL Supply Voltage	4V			
Reference Frequency voltage	3.6Vp-p			
Data, Clock & LE levels	3.3V			

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS					
RF OUT	7	CLOCK	10		
VCC VCO	5	DATA	11		
VCC PLL	1	LATCH ENABLE	12		
REF IN	3	GROUND	2,4,6,8,13,14		
LOCK DETECT	9				

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