## Engineering Development Model

## **Frequency Synthesizer**

## KSN-EDR11011SA

## **Important Note**

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



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**CASE STYLE: DK1042** 

ELECTRICAL SPECIFICATIONS 50Ω, over -5°C to +75°C						
Parameter	Min	Тур.	Max.	Units		
Frequency	100		100	MHz		
Step size	. 0	10000		kHz		
Settling Time Within ±1kHz		250		μsec		
Output Power	+1	+5 🦰	+9	dBm		
Phase Noise at 100 Hz offse		111	•	dBc/Hz		
at 1 kHz offse		122	-117	dBc/Hz		
at 10 KHz offse	t	-124	-111	dBc/Hz		
at 100 KHz offse		-136	-131	dBc/Hz		
at 1000 kHz offse	t	-159	-153	dBc/Hz		
Integrated SSB Phase Noise	4. C1	-75		dBc		
Ref & Comp Spurious Suppression	1.10	-88		dBc		
Non-Harm. Spurious Suppression		-90		dBc		
Harmonic Suppression		-23		dBc		
Supply voltage VCO	8	5		V V		
Supply current VCO PLL		36 4	44 12	V V		
Frequency		10		MHz		
Reference In Amplitude	40	1		Vp-p		
(External) Impedance		100		kΩ		
Ph. N @ 1kHz		-145		dBc/Hz		
Input Logic Logic high	2.4		3	V		
Levels Logic Low			0.6	V		
Digital Lock Locked	2.6		3	V		
Detect Unlocked			0.4	V		
Frequency Synthesizer PLL ADF4001						

ABSOLUTE MAXIMUM RATINGS				
Operating Temperature	-45°C to 85°C			
Storage Temperature	-55°C to 100°C			
VCO Supply Voltage	6V			
PLL Supply Voltage	4V			
Reference Frequency voltage	5.8Vp-p			
Data, Clock & LE levels	3.3V			

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS					
RF OUT	7	CLOCK	10		
VCC VCO	5	DATA	11		
VCC PLL	1	LATCH ENABLE	12		
REF IN	3	GROUND	2,4,6,8,13,14		
LOCK DETECT	9				

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