

Engineering Development Model

Frequency Synthesizer

KSN-EDR7450/1

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



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CASE STYLE : DK1042

ELECTRICAL SPECIFICATIONS 50Ω, over -45°C to +85°C				
Parameter	Min.	Typ.	Max.	Units
Frequency	1667		1747	MHz
Step size		100		kHz
Settling Time Within ±50Hz		2.5		msec
Output Power	-2	+3	+6	dBm
Phase Noise				
at 100 Hz offset		-75		dBc/Hz
at 1 kHz offset		-75		dBc/Hz
at 10 kHz offset		-86		dBc/Hz
at 100 kHz offset		-121		dBc/Hz
at 1000 kHz offset		-147		dBc/Hz
Integrated SSB Phase Noise		-35		dBc
Reference Spurious Suppression		-98		dBc
Comparison Spurious Suppression		-119		dBc
Non-Harm. Spurious Suppression		-90		dBc
Harmonic Suppression		-56		dBc
Supply voltage VCO		5		V
Supply voltage PLL		5		V
Supply current VCO		27	35	mA
Supply current PLL		5	13	mA
Reference In (External)				
Frequency		10		MHz
Amplitude		1		Vp-p
Impedance		100		kΩ
Ph. N @ 1kHz		-145		dBc/Hz
Input Logic Levels				
Logic high	4		5	V
Logic Low			1	V
Digital Lock Detect				
Locked	4.6		5	V
Unlocked			0.4	V
Frequency Synthesizer PLL		LMX2326		

ABSOLUTE MAXIMUM RATINGS	
Operating Temperature	-45°C to 85°C
Storage Temperature	-55°C to 100°C
VCO Supply Voltage	6V
PLL Supply Voltage	6V
Reference Frequency voltage	5.8Vp-p
Data, Clock & LE levels	5.3V

Power On sequence: Vcc VCO followed by Vcc PLL

Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS			
RF OUT	3	CLOCK	10
VCC VCO	5	DATA	11
VCC PLL	1	LATCH ENABLE	12
REF IN	7	GROUND	2,4,6,8,13,14
LOCK DETECT	9		

Notes

- A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
 B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuits' applicable established test performance criteria and measurement instructions.
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