Engineering Development Model

Frequency Synthesizer

KSN-EDR7656/2

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



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CASE STYLE: DK1042

ELECTRICAL SPECIFICATIONS 50Ω, over -45°C to +85°C						
Parameter	Min.	Тур.	Max.	Units		
Frequency	720		793	MHz		
Step size	A 2	100		kHz		
Settling Time Within ±50Hz		3.5		msec		
Output Power	-3	+1	+5	₫Bm		
Phase Noise at 100 Hz offs at 1 kHz offs	set	-86 -83		dBc/Hz dBc/Hz		
at 10 KHz offs at 100 KHz offs at 1000 kHz offs	set	-96 -117 -144	100	dBc/Hz dBc/Hz dBc/Hz		
Integrated SSB Phase Noise		-42		dBc		
Reference Spurious Suppression		-92		dBc		
Comparison Spurious Suppression		-116		dBc		
Non-Harm. Spurious Suppression	A	-90		dBc		
Harmonic Suppression		-35	-26	dBc		
Supply voltage VCO PLL	0	5		V V		
Supply current VCO PLL		25 8	33 16	mA mA		
Frequency Reference in Amplitude (External) Impedance Ph. N @ 1kHz	140	10 1 100 -145		MHz Vp-p kΩ dBc/Hz		
Input Logic Logic high Logic Low	4		5 1	V		
Digital Lock Locked Detect Unlocked	4.6		5 0.4	V		
Frequency Synthesizer PLL		ADF41	18			

ABSOLUTE MAXIMUM RATINGS				
Operating Temperature	-45°C to 85°C			
Storage Temperature	-55°C to 100°C			
VCO Supply Voltage	6V			
PLL Supply Voltage	6V			
Reference Frequency voltage	5.8Vp-p			
Data, Clock & LE levels	5.3V			

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS				
RF OUT	3	CLOCK	10	
VCC VCO	5	DATA	11	
VCC PLL	1	LATCH ENABLE	12	
REF IN	7	GROUND	2,4,6,8,13,14	
LOCK DETECT	9			