Engineering Development Model

Frequency Synthesizer KSN-EDR8050

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability.
At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.

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CASE STYLE : DK801

ELECTRICAL SPECIFICATIONS 50Ω, over -45°C to +85°C					
Parameter		**Min.**	**Typ.**	**Max.**	**Units**
Frequency		639		645	MHz
Step size			20		kHz
Settling Time	Within ±1kHz		5.5		msec
Output Power		-4	0	+4	dBm
Phase Noise					
	at 100 Hz offset		-74		dBc/Hz
	at 1 kHz offset		-79		dBc/Hz
	at 10 KHz offset		-112	-106	dBc/Hz
	at 100 KHz offset		-138	-133	dBc/Hz
	at 1000 kHz offset		-159	-153	dBc/Hz
Integrated SSB Phase Noise			-42		dBc
Reference Spurious Suppression			-102		dBc
Comparison Spurious Suppression			-119		dBc
Non-Harm. Spurious Suppression			-90		dBc
Harmonic Suppression			-21		dBc
Supply voltage	VCO		5		V
	PLL		5		V
Supply current	VCO		12	21	mA
	PLL		4	12	mA
Reference In (External)	Frequency		10		MHz
	Amplitude		1		Vp-p
	Impedance		100		kΩ
	Ph. N @ 1kHz		-145		dBc/Hz
Input Logic Levels	Logic high	4		5	V
	Logic Low			1	
Digital Lock Detect	Locked	4.6		5	V
	Unlocked			0.4	
Frequency Synthesizer PLL			ADF4118		

ABSOLUTE MAXIMUM RATINGS	
Operating Temperature	-45°C to 85°C
Storage Temperature	-55°C to 100°C
VCO Supply Voltage	6V
PLL Supply Voltage	6V
Reference Frequency voltage	5.8Vp-p
Data, Clock & LE levels	5.3V

Power On sequence: Vcc VCO followed by Vcc PLL
Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS			
RF OUT	7	CLOCK	10
VCC VCO	5	DATA	11
VCC PLL	1	LATCH ENABLE	12
REF IN	3	GROUND	2,4,6,8,13,14
LOCK DETECT	9		