Engineering Development Model

Frequency Synthesizer

KSN-EDR8461/2

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



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CASE STYLE: DK801

ELECTRICAL SPECIFICATIONS 50Ω, over -45°C to +85°C						
Parameter		Min.	Тур.	Max.	Units	
Frequency		2022		2123	MHz	
Step size			50		kHz	
Settling Time Within ±1kHz			14		msec	
Output Power		+2	+6	+9	₫₿m	
Phase Noise	at 100 Hz offset at 1 kHz offset		67 -72		dBc/Hz dBc/Hz	
	at 10 KHz offset at 100 KHz offset at 1000 kHz offset		-99 -122 -142	-94 -117 -137	dBc/Hz dBc/Hz dBc/Hz	
Integrated SSB Phase Noise			-42		dBc	
Reference Spurious Suppression			-93		dBc	
Comparison Spurious Suppression			-109		dBc	
Non-Harm. Spurious Suppression			-90		dBc	
Harmonic Suppression			-25		dBc	
Supply voltage	VCO PLL		5 3.3		V V	
Supply current	VCO PLL		44 10	52 18	mA mA	
,	Frequency Amplitude Impedance	. 40	24 1 100		MHz Vp-p kΩ	
Input Logic Levels	h. N @ 1kHz Logic high Logic Low	2.64	-145	3.3 0.66	dBc/Hz V	
Digital Lock Detect	Locked Unlocked	2.9		3.3 0.4	V	
Frequency Synthesizer PLL		ADF4118				

ABSOLUTE MAXIMUM RATINGS					
Operating Temperature	-45°C to 85°C				
Storage Temperature	-55°C to 100°C				
VCO Supply Voltage	6V				
PLL Supply Voltage	4.3V				
Reference Frequency voltage	5.8Vp-p				
Data, Clock & LE levels	3.6V				

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS					
RF OUT	3	CLOCK	10		
VCC VCO	5	DATA	11		
VCC PLL	1	LATCH ENABLE	12		
REF IN	7	GROUND	2,4,6,8,13,14		
LOCK DETECT	9				