Engineering Development Model

Frequency Synthesizer

KSN-EDR8979

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply final specification sheet, part number and price/delivery information.



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CASE STYLE: DK801

ELECTRICAL SPECIFICATIONS 50Ω, over -45°C to +85°C						
Parameter		Min.	Тур.	Max.	Units	
Frequency		866		885	MHz	
Step size			1000		kHz	
Settling Time Within ±1kHz			3.5		msec	
Output Power		-3	+1	+5	₫Bm	
Phase Noise						
á	at 100 Hz offset		-91		dBc/Hz	
	at 1 kHz offset		-91		dBc/Hz	
а	t 10 KHz offset		-109		dBc/Hz	
	100 KHz offset		-137	-131	dBc/Hz	
	1000 kHz offset		-156	-151	dBc/Hz	
Integrated SSB Phase Noise			-54		dBc	
Reference Spurious Suppression			-95		dBc	
Comparison Spurious Suppression			-103		dBc	
Non-Harm. Spurious Suppression			-90		dBc	
Harmonic Suppression	9		-28	-22	dBc	
Supply voltage	vco		5		V	
ouppy to augo	PLL		5		V	
Supply current	VCO		34	42	mA	
	PLL		11	20	mA	
	equency	.10	15		MHz	
	nplitude		1		Vp-p	
	pedance		100		kΩ	
	N @ 1kHz		-145		dBc/Hz	
	gic high	4		5	V	
Levels Logic Low				1	•	
J	.ocked	4.6		5	V	
Detect Unlocked				0.4	•	
Frequency Synthesizer PLL		ADF4113				

ABSOLUTE MAXIMUM RATINGS					
Operating Temperature	-45°C to 85°C				
Storage Temperature	-55°C to 100°C				
VCO Supply Voltage	6V				
PLL Supply Voltage	6V				
Reference Frequency voltage	5.8Vp-p				
Data, Clock & LE levels	5.3V				

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS					
RF OUT	7	CLOCK	10		
VCC VCO	5	DATA	11		
VCC PLL	1	LATCH ENABLE	12		
REF IN	3	GROUND	2,4,6,8,13,14		
LOCK DETECT	9				