

# Engineering Development Model

## Frequency Synthesizer

KSN-EDR9230/1

### Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



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CASE STYLE : DK1042

| ELECTRICAL SPECIFICATIONS 50Ω, over -45°C to +85°C |      |         |      |        |
|----------------------------------------------------|------|---------|------|--------|
| Parameter                                          | Min. | Typ.    | Max. | Units  |
| Frequency                                          | 3244 |         | 3444 | MHz    |
| Step size                                          |      | 250     |      | kHz    |
| Settling Time Within ±1kHz                         |      | 40      |      | msec   |
| Output Power                                       | -3   | +1      | +5   | dBm    |
| Phase Noise                                        |      |         |      |        |
| at 100 Hz offset                                   |      | -79     |      | dBc/Hz |
| at 1 kHz offset                                    |      | -87     |      | dBc/Hz |
| at 10 KHz offset                                   |      | -92     | -87  | dBc/Hz |
| at 100 KHz offset                                  |      | -118    | -113 | dBc/Hz |
| at 1000 kHz offset                                 |      | -138    | -134 | dBc/Hz |
| Integrated SSB Phase Noise                         |      | -47     |      | dBc    |
| Ref & Comp Spurious Suppression                    |      | -96     |      | dBc    |
| 0.5 Step size Spurious Suppression                 |      | -106    |      | dBc    |
| Non-Harm. Spurious Suppression                     |      | -90     |      | dBc    |
| Harmonic Suppression                               |      | -34     |      | dBc    |
| Supply voltage VCO                                 |      | 5       |      | V      |
| Supply voltage PLL                                 |      | 3       |      | V      |
| Supply current VCO                                 |      | 53      | 61   | mA     |
| Supply current PLL                                 |      | 21      | 29   | mA     |
| Reference In (External) Frequency                  |      | 30      |      | MHz    |
| Reference In (External) Amplitude                  |      | 1       |      | Vp-p   |
| Reference In (External) Impedance                  |      | 100     |      | kΩ     |
| Reference In (External) Ph. N @ 1kHz               |      | -145    |      | dBc/Hz |
| Input Logic Levels Logic high                      | 1.4  |         | 3    | V      |
| Input Logic Levels Logic Low                       |      |         | 0.6  | V      |
| Digital Lock Detect Locked                         | 1.4  |         | 3    | V      |
| Digital Lock Detect Unlocked                       |      |         | 0.4  | V      |
| Frequency Synthesizer PLL                          |      | ADF4153 |      |        |

| ABSOLUTE MAXIMUM RATINGS    |                |
|-----------------------------|----------------|
| Operating Temperature       | -45°C to 85°C  |
| Storage Temperature         | -55°C to 100°C |
| VCO Supply Voltage          | 6V             |
| PLL Supply Voltage          | 4V             |
| Reference Frequency voltage | 3.6Vp-p        |
| Data, Clock & LE levels     | 3.3V           |

Power On sequence: Vcc VCO followed by Vcc PLL

Power Off sequence: Vcc PLL followed by Vcc VCO

| PIN CONNECTIONS |   |              |               |
|-----------------|---|--------------|---------------|
| RF OUT          | 7 | CLOCK        | 10            |
| VCC VCO         | 5 | DATA         | 11            |
| VCC PLL         | 1 | LATCH ENABLE | 12            |
| REF IN          | 3 | GROUND       | 2,4,6,8,13,14 |
| LOCK DETECT     | 9 |              |               |

### Notes

- A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.  
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[www.minicircuits.com](http://www.minicircuits.com) P.O. Box 350168, Brooklyn, NY 11235-0003 (718) 934-4500 sales@minicircuits.com

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