Engineering Development Model

Frequency Synthesizer

KSN-EDR9428

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



Please click "Back", and then click "Contact Us" for Applications support.

CASE STYLE: DK1042

ELECTRICAL SPECIFICATIONS 50Ω, over -25°C to +55°C						
Parameter	Min.	Тур.	Max.	Units		
Frequency	2037.28		2037.28	MHz		
Step size		2140		kHz		
Settling Time Within ±1kHz		8		msec		
Output Power	-3	0	+4	₫₿m		
Phase Noise at 100 Hz	offset	-82		dBc/Hz		
at 1 kHz at 10 KHz	offset	-92 -99	-86 -94	dBc/Hz dBc/Hz		
at 100 KHz at 1000 kHz		-127 -148	-122 -142	dBc/Hz dBc/Hz		
Integrated SSB Phase Noise		-49		dBc		
Ref & Comp Spurious Suppression		-105		dBc		
0.5 Step size Spurious Suppression		-113		dBc		
Non-Harm. Spurious Suppression 👍		-90		dBc		
Harmonic Suppression		-33	-26	dBc		
Supply voltage VCO PLL	4 0	5		V V		
Supply current VCO PLL		44 14	52 22	mA mA		
Reference In Frequency Amplitude	. 40	10.7		MHz Vp-p		
(External) Impedance Ph. N @ 1kHz		100 -145		kΩ dBc/Hz		
Input Logic Logic high Levels Logic Low	1.4		3 0.6	V		
Digital Lock Locked Detect Unlocked	1 1 1 1 1 1 1 1 1 1		3 0.4	V		
Frequency Synthesizer PLL		ADF41	53	-		

ABSOLUTE MAXIMUM RATINGS				
Operating Temperature	-45°C to 85°C			
Storage Temperature	-55°C to 100°C			
VCO Supply Voltage	6V			
PLL Supply Voltage	4V			
Reference Frequency voltage	3.6Vp-p			
Data, Clock & LE levels	3.3V			

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS					
RF OUT	7	CLOCK	10		
VCC VCO	5	DATA	11		
VCC PLL	1	LATCH ENABLE	12		
REF IN	3	GROUND	2,4,6,8,13,14		
LOCK DETECT	9				