Engineering Development Model

Frequency Synthesizer KSN-EDR9435/2

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability.
At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.

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CASE STYLE : DK1042

ELECTRICAL SPECIFICATIONS 50Ω, over -45°C to +85°C					
Parameter		**Min.**	**Typ.**	**Max.**	**Units**
Frequency		2151.76		2302.84	MHz
Step size			20		kHz
Settling Time	Within ±1kHz		35		msec
Output Power		+2	+5	+9	dBm
Phase Noise					
	at 100 Hz offset		-77		dBc/Hz
	at 1 kHz offset		-83		dBc/Hz
	at 10 KHz offset		-99		dBc/Hz
	at 100 KHz offset		-127	-121	dBc/Hz
	at 1000 kHz offset		-147	-141	dBc/Hz
Integrated SSB Phase Noise			-48		dBc
Reference Spurious Suppression			-103		dBc
Comparison Spurious Suppression			-102		dBc
0.5 Step size Spurious Suppression			-82		dBc
Non-Harm. Spurious Suppression			-90		dBc
Harmonic Suppression			-38		dBc
Supply voltage	**VCO**		5		V
	PLL		5		V
Supply current	**VCO**		44	53	mA
	PLL		39	48	mA
Reference In (External)	**Frequency**		30.72		MHz
	Amplitude		1		Vp-p
	Impedance		100		kΩ
	Ph. N @ 1kHz		-145		dBc/Hz
Input Logic Levels	**Logic high**	1.4		3.6	V
	Logic Low			0.6	
Digital Lock Detect	**Locked**	1.4		3.6	V
	Unlocked			0.4	
Frequency Synthesizer PLL			ADF4153		

ABSOLUTE MAXIMUM RATINGS	
Operating Temperature	-45°C to 85°C
Storage Temperature	-55°C to 100°C
VCO Supply Voltage	6V
PLL Supply Voltage	6V
Reference Frequency voltage	3.6Vp-p
Data, Clock & LE levels	3.9V

Power On sequence: Vcc VCO followed by Vcc PLL
Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS			
RF OUT	7	**CLOCK**	10
VCC VCO	5	**DATA**	11
VCC PLL	1	**LATCH ENABLE**	12
REF IN	3	**GROUND**	2,4,6,8,13,14
LOCK DETECT	9		