Engineering Development Model

Frequency Synthesizer KSN-EDR9543

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability.
At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.

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CASE STYLE : DK1042

ELECTRICAL SPECIFICATIONS 50Ω, over -45°C to +85°C				
Parameter	**Min.**	**Typ.**	**Max.**	**Units**
Frequency	2011		2031	MHz
Step size		125		kHz
Settling Time Within ±1kHz		18		msec
Output Power	0	+4	+7	dBm
Phase Noise				
at 100 Hz offset		-61		dBc/Hz
at 1 kHz offset		-78		dBc/Hz
at 10 KHz offset		-107	-101	dBc/Hz
at 100 KHz offset		-130	-124	dBc/Hz
at 1000 kHz offset		-150	-145	dBc/Hz
Integrated SSB Phase Noise		-30		dBc
Reference Spurious Suppression		-103		dBc
Comparison Spurious Suppression		-123		dBc
Non-Harm. Spurious Suppression		-90		dBc
Harmonic Suppression		-39		dBc
Supply voltage VCO		5		V
Supply voltage PLL		3.3		V
Supply current VCO		48	56	mA
Supply current PLL		8	16	mA
Reference In (External) Frequency		20		MHz
Reference In (External) Amplitude		1		Vp-p
Reference In (External) Impedance		100		kΩ
Reference In (External) Ph. N @ 1kHz		-145		dBc/Hz
Input Logic Levels Logic high	2.64		3.3	V
Input Logic Levels Logic Low			0.66	
Digital Lock Detect Locked	2.9		3.3	V
Digital Lock Detect Unlocked			0.4	
Frequency Synthesizer PLL	ADF4118			

ABSOLUTE MAXIMUM RATINGS	
Operating Temperature	-45°C to 85°C
Storage Temperature	-55°C to 100°C
VCO Supply Voltage	6V
PLL Supply Voltage	4.3V
Reference Frequency voltage	5.8Vp-p
Data, Clock & LE levels	3.6V

Power On sequence: Vcc VCO followed by Vcc PLL
Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS			
RF OUT	3	**CLOCK**	10
VCC VCO	5	**DATA**	11
VCC PLL	1	**LATCH ENABLE**	12
REF IN	7	**GROUND**	2,4,6,8,13,14
LOCK DETECT	9		