## Engineering Development Model

## **Frequency Synthesizer**

## KSN-EDR9658

## **Important Note**

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



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**CASE STYLE: DK1042** 

ELECTRICAL SPECIFICATIONS 50Ω, over -45°C to +85°C						
Parameter		Min.	Тур.	Max.	Units	
Frequency		3230		3480	MHz	
Step size			250		kHz	
Settling Time Within ±1kHz		5	16		msec	
Output Power		-2	+2	+6	dBm	
Phase Noise	at 100 Hz offset at 1 kHz offset at 10 KHz offset		-76 -83 -89	-78 -83	dBc/Hz dBc/Hz dBc/Hz	
	at 100 KHz offset at 1000 kHz offset		-83 -1 <b>37</b>	-110	dBc/Hz dBc/Hz	
Integrated SSB Phase Noise			-43		dBc	
Ref & Comp Spurious Suppression			-86		dBc	
0.5 Step size Spurious Suppression			-106		dBc	
Non-Harm. Spurious Suppression		40 >	-90	Ť	dBc	
Harmonic Suppression			-26		dBc	
Supply voltage	VCO PLL		5		V V	
Supply current	VCO PLL	10	39 20	48 28	mA mA	
	Frequency Amplitude Impedance Ph. N @ 1kHz		30 1 100 -145		MHz Vp-p kΩ dBc/Hz	
Input Logic Levels	Logic high Logic Low	1.4		3 0.6	V	
Digital Lock Detect	Locked Unlocked	1.4		3 0.4	V	
Frequency Synthesizer PLL		ADF4153				

ABSOLUTE MAXIMUM RATINGS					
Operating Temperature	-45°C to 85°C				
Storage Temperature	-55°C to 100°C				
VCO Supply Voltage	6V				
PLL Supply Voltage	4V				
Reference Frequency voltage	3.6Vp-p				
Data, Clock & LE levels	3.3V				

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS					
RF OUT	7	CLOCK	10		
VCC VCO	5	DATA	11		
VCC PLL	1	LATCH ENABLE	12		
REF IN	3	GROUND	2,4,6,8,13,14		
LOCK DETECT	9				