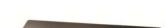
Engineering Development Model

Frequency Synthesizer

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



KSN-EDR9694



Please click "Back", and then click "Contact Us" for Applications support.

CASE STYLE: DK1171

ELECTRICAL SPECIFICATIONS 50Ω, over -45°C to +85°C						
Parameter		Min.	Тур.	Max.	Units	
Frequency		2168		2232	MHz	
Step size			100		kHz	
Settling Time Within ±1kHz			11		msec	
Output Power		-1	+3	+7	₫₿m	
Phase Noise						
	at 100 Hz offset		-72		dBc/Hz	
	at 1 kHz offset		-78		dBc/Hz	
	at 10 KHz offset		-110		dBc/Hz	
	at 100 KHz offset		-133		dBc/Hz	
	at 1000 kHz offset		-153		dBc/Hz	
Integrated SSB Phase Noise			-40		dBc	
Reference Spurious Suppression			-99		dBc	
Comparison Spurious Suppression			-42		dBc	
Non-Harm. Spurious Suppression			-90		dBc	
Harmonic Suppression	<u> </u>		-37		dBc	
Supply voltage	VCO		5		V	
Supply Voltage	PLL		5		V	
Supply current	vco		31	39	mA	
oupply current	PLL		16	24	mA	
. 0	Frequency	.10	10		MHz	
Reference In	Amplitude	. 4	1		Vp-p	
(External)	Impedance		100		kΩ	
	Ph. N @ 1kHz		-145		dBc/Hz	
Input Logic	Logic high	4		5	V	
Levels	Logic Low			1	•	
Digital Lock	Locked	4.6		5	V	
Detect	Unlocked			0.4	•	
Frequency Synthesizer PLL			ADF4113			

ABSOLUTE MAXIMUM RATINGS					
Operating Temperature	-45°C to 85°C				
Storage Temperature	-55°C to 100°C				
VCO Supply Voltage	6V				
PLL Supply Voltage	6V				
Reference Frequency voltage	5.8Vp-p				
Data, Clock & LE levels	5.3V				

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS					
RF OUT	7	CLOCK	10		
VCC VCO	5	DATA	11		
VCC PLL	1	LATCH ENABLE	12		
REF IN	3	GROUND	2,4,6,8,13,14		
LOCK DETECT	9				