Engineering Development Model

Frequency Synthesizer KSN-EDR97331MP

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability.
At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.

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CASE STYLE : DK1042

ELECTRICAL SPECIFICATIONS 50Ω, over -40°C to +70°C					
Parameter		**Min.**	**Typ.**	**Max.**	**Units**
Frequency		3000		3500	MHz
Step size			1000		kHz
Settling Time	Within ±1kHz		400		µsec
Output Power		-1	+4	+8	dBm
Phase Noise					
	at 100 Hz offset		-81		dBc/Hz
	at 1 kHz offset		-90		dBc/Hz
	at 10 KHz offset		-96		dBc/Hz
	at 100 KHz offset		-96	-90	dBc/Hz
	at 1000 kHz offset		-126		dBc/Hz
Integrated SSB Phase Noise			-43		dBc
Ref & Comp Spurious Suppression			-101		dBc
0.5 Step size Spurious Suppression			-63		dBc
Non-Harm. Spurious Suppression			-90		dBc
Harmonic Suppression			-38		dBc
Supply voltage	VCO		7		V
	PLL		3		V
Supply current	VCO		40	50	V
	PLL		13	22	V
Reference In (External)	Frequency		10		MHz
	Amplitude		1		Vp-p
	Impedance		100		kΩ
	Ph. N @ 1kHz		-145		dBc/Hz
Input Logic Levels	Logic high	1.4		3	V
	Logic Low			0.6	
Digital Lock Detect	Locked	1.4		3	V
	Unlocked			0.4	
Frequency Synthesizer PLL		ADF4153			

ABSOLUTE MAXIMUM RATINGS	
Operating Temperature	-45°C to 85°C
Storage Temperature	-55°C to 100°C
VCO Supply Voltage	8V
PLL Supply Voltage	4V
Reference Frequency voltage	3.6Vp-p
Data, Clock & LE levels	3.3V

Power On sequence: Vcc VCO followed by Vcc PLL
Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS			
RF OUT	7	**CLOCK**	10
VCC VCO	5	**DATA**	11
VCC PLL	1	**LATCH ENABLE**	12
REF IN	3	**GROUND**	2,4,6,8,13,14
LOCK DETECT	9		