

Super Wideband Monolithic Amplifier Die

LTA-183M-D+

50Ω DC to 18 GHz

The Big Deal

- Super Wideband, DC to 18 GHz
- Good P1dB, 23.2dBm at 10 GHz
- Good OIP3, 29.5dBm at 10 GHz
- Good Directivity, 27 dB typ.



Product Overview

The LTA-183M-D+ is a super wideband distributed amplifier die that operates from DC to 18 GHz fabricated using PHEMT process. It delivers excellent gain flatness, good return loss, medium current with good P1dB and OIP3 across a wide bandwidth without the need of external matching network. It has high active directivity enabling to replace expensive isolators in most applications.

Key Features

Feature	Advantages
Super Wideband: DC to 18 GHz <ul style="list-style-type: none">• 20.4 dB Gain at 50 MHz• 14.2 dB Gain at 18 GHz	General purpose wideband amplifier is suitable for various applications including HF, VHF thru KU band.
Good P1dB & OIP3 <ul style="list-style-type: none">• 23.2 dBm P1dB at 10 GHz• 29.5 dBm OIP3 at 10 GHz	Suitable as a driver amplifier in receiver/transmitter chains.
Good Directivity, 27 dB typ.	Isolates adjacent circuitry without need for an external expensive isolator.
Good input and output return loss	Eliminates need for external matching circuit providing published return loss.
Unpackaged die	Enables user to integrate it directly into hybrids.

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- Gain, 14.5dB at 10GHz
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- OIP3, 29.5dBm at 10GHz

Typical Applications

- Instrumentation
- Cellular Infrastructure
- Defense
- Test & Measurement



+RoHS Compliant

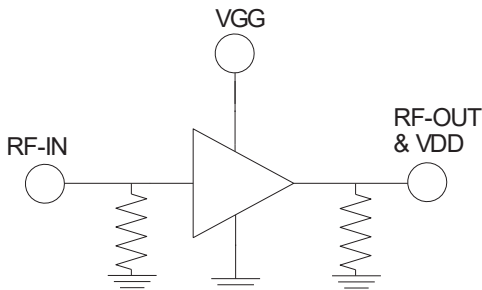
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Ordering Information: Refer to Last Page

General Description

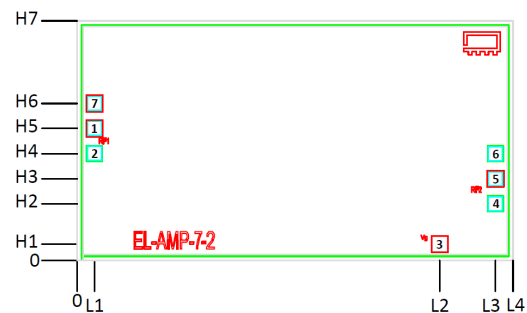
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Simplified Schematic and Pad description



Pad #	Description
1	RF-IN
3	V _{GG}
5	RF-OUT & V _{DD}
2,4,6,7 & Bottom of Die	GROUND

Bonding Pad Position



Dimensions in μm, Typical

L1	L2	L3	L4	H1	H2	H3	H4	H5	H6	H7
103	2174	2508	2614	98	340	490	640	793	943	1438

Thickness	Die size	Pad size 1,2,4,5, 6 & 7	Pad size 3
100	2614 x 1438	85 x 85	93 x 93

Electrical Specifications at 25°C, $V_{DD}=8V$, $I_{DD}=160mA$ & $Z_o=50\Omega$ unless noted

Parameter	Condition (MHz)	$V_{DD}=8V^1$			Units
		Min.	Typ.	Max.	
Frequency Range ¹		0.05		18	GHz
Gain	50		20.4		dB
	5000		15.9		
	10000		14.5		
	15000		14.6		
	18000		14.2		
Input Return Loss	50		10		dB
	5000		22		
	10000		14		
	15000		11		
	18000		10		
Output Return Loss	50		9		dB
	5000		17		
	10000		19		
	15000		18		
	18000		21		
Directivity	50 - 18000		27		dB
Output Power at 1dB Compression ²	50		25.4		dBm
	5000		24.4		
	10000		23.2		
	15000		22.9		
	18000		22.9		
Output IP3 ($P_{out} = 5dBm/Tone$)	50		38.6		dBm
	5000		33.4		
	10000		29.5		
	15000		26.8		
	18000		25.2		
Noise Figure	50		5.4		dB
	5000		2.0		
	10000		2.8		
	15000		3.5		
	18000		4.4		
Device Operating Voltage (V_{DD})			8		V
Device Operating Current (I_{DD})		—	160	—	mA
Device Gate Voltage (V_{GG})			-1.3		V
Device Gate Current (I_{GG})			-0.5		mA
Thermal Resistance, junction-to-ground lead			17.3		°C/W

1. Die is tested in die characterization board. See characterization circuit (Fig. 1). Starting frequency of this device is dependent on the input blocking capacitor value.

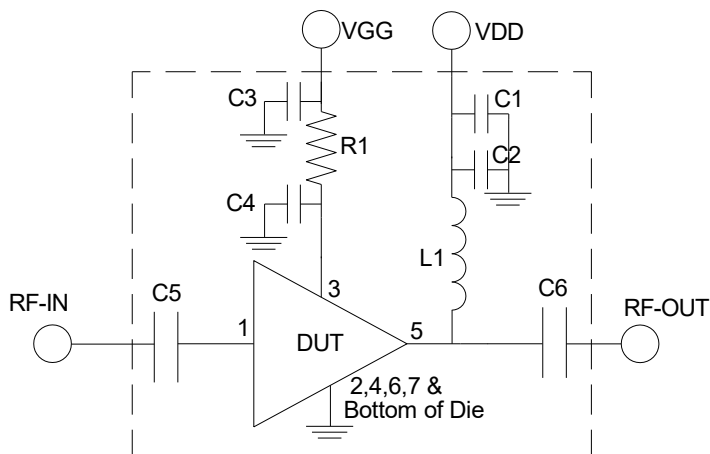
2. DC current increases to 258mA typ. at P1dB.

Absolute Maximum Ratings³

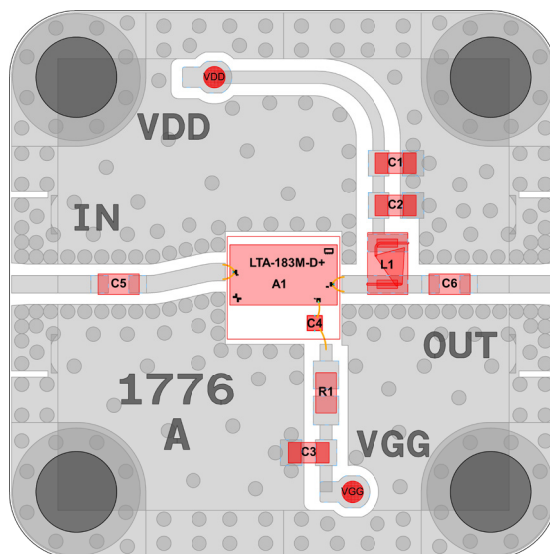
Parameter	Ratings
Operating Temperature (ground lead)	-40°C to 85°C
Junction Temperature	150°C
Total Power Dissipation	2.8W
Input Power (CW)	21dBm
DC Voltage on RF-OUT & V_{DD}	14V
DC Voltage on V_{GG}	-2V to -0.5V
Current I_{DD}	350mA
Current I_{GG}	-1.5mA to 0mA

3. Permanent damage may occur if these limits are exceeding.

Characterization & Application Test Circuit



Assembly Diagram



Component	Value	Size	Part Number	Manufacturer
C2, C3, C5 & C6	0.1uF	0402	0402BB104KG500	Passive Plus
C4	100pF	15 x 15mil	LSA1515B101M2H5C-F	Presidio
C1	NA	NA	Not Used	NA
L1	0.17uH	60 x 40mil	CC20T44K240G5-C	Piconics
R1	1kOhm	0402	RR0510P-102-D	Susumu
A1	NA	2614um x1438um	LTA-183M-D+	Mini-Circuits

Fig 1. Characterization & Application Test Circuit

Note: This block diagram is used for characterization. (Die is attached and wire-bonded on die characterization test board. Gain, Return loss, Output power at 1dB compression (P1dB), output IP3 (OIP3) and noise figure are measured using Agilent's N5242A PNA-X microwave network analyzer.

Conditions:

- 1.VDD=8V
- 2.VG is set to obtain desired IDD as shown in specification table.
- 3.Gain and Return loss: Pin= -25dBm
- 4.Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 5 dBm/tone at output.


Power ON Sequence:

- 1) Turn on VGG =-1.8V
- 2) Turn on VDD = 8V
- 3) Adjust VGG until IDD=160mA (Typically, VGG = -1.3V)

Power OFF Sequence:

- 1) Turn back VGG = -1.8V
- 2) Turn off VDD
- 3) Turn off VGG

Assembly and Handling Procedure

1. **Storage**
Dice should be stored in a dry nitrogen purged desiccators or equivalent.
2.  **ESD**
MMIC PHEMT amplifier dice are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic protected material, which should be open in clean room conditions at an appropriately grounded anti-static workstation.
3. **Die Handling and Attachment**
Devices need careful handling using correctly designed collets, it is recommended to handle the chip along the edges with a custom design collet. The die mounting surface must be clean and flat. Using conductive silver filled epoxy, recommended epoxies are Ablestik 84-1 LMISR4 or equivalents. Apply sufficient epoxy to meet required epoxy bond line thickness, epoxy fillet height and epoxy coverage around total periphery. Parts shall be cured in a nitrogen filled atmosphere per manufacturer's cure condition. The surface of the chip has exposed air bridges and should not be touched with vacuum collet, tweezers or fingers.
5. **Wire Bonding**
Bond pad openings in the surface passivation above the bond pads are provided to allow wire bonding to the dice gold bond pads. Thermo-sonic bonding is used with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. Suggested wire is pure gold, 1mil diameter. Bonds must be made from the bond pads on the die to the packaged or substrate. All bond wires should be kept as short as low as reasonable to minimize performance degradation due to undesirable series inductance.

Additional Detailed Technical Information <i>additional information is available on our dash board.</i>							
Performance Data	Data Table						
	Swept Graphs						
	S-Parameter (S2P Files) Data Set with and without port extension(.zip file)						
Case Style	Die						
Die Ordering and packaging information	<table> <tr> <td>Quantity, Package</td> <td>Model No.</td> </tr> <tr> <td>Small, Gel - Pak: 5,10,50,100 KGD*</td> <td>LTA-183M-DG+</td> </tr> <tr> <td>Medium†, Partial wafer: KGD*<570</td> <td>LTA-183M-DP+</td> </tr> </table> <p>†Available upon request contact sales representative</p> <p>Refer to AN-60-067</p>	Quantity, Package	Model No.	Small, Gel - Pak: 5,10,50,100 KGD*	LTA-183M-DG+	Medium†, Partial wafer: KGD*<570	LTA-183M-DP+
Quantity, Package	Model No.						
Small, Gel - Pak: 5,10,50,100 KGD*	LTA-183M-DG+						
Medium†, Partial wafer: KGD*<570	LTA-183M-DP+						
Die TB Reference	XM-C9A1-0404D (Please check X-Microwave's Website)						
Environmental Ratings	ENV80						

*Known Good Dice ("KGD") means that the dice are taken from PCM good wafer and visually inspected in question have been subjected to Mini-Circuits while this is not definitive, it does help to provide a higher degree of confidence that dice are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

Additional Notes

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