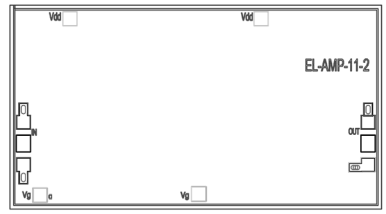
Super Wideband, Flat Gain

Monolithic Amplifier Die

LTA-2183-D+

50Ω   2 to 18 GHz



The Big Deal

- Super Wideband, 2 to 18 GHz
- Flat Gain 16.6±0.7 dB from 2 to 18 GHz
- Good P1dB, 19.6 dBm at 10 GHz
- Good OIP3, +27.4 dBm at 10 GHz
- Good Directivity, 47.4 dB typ.

Product Overview

LTA-2183-D+ is an amplifier die that operates from 2 to 18GHz that is fabricated on a GaAs PHEMT MMIC process. The Amplifier provides 16.6dB of Gain, 27.6dBm OIP3 and 19.7dBm output power at 1dB compression point with 16dB typical return loss while requiring 4V and 210mA DC power. Gain flatness is +/- 0.7dB across the operating bandwidth. The Amplifier is ideal for use in very wideband ECM, Test & Measurement and Microwave communications systems.

Key Features

Feature	Advantages
Super Wideband: 2 to 18 GHz • 15.9 dB Gain at 2 GHz • 16.9 dB Gain at 18 GHz	General purpose wideband amplifier is suitable for various applications
Good P1dB & OIP3 • 19.6 dBm P1dB at 10 GHz • 27.4 dBm OIP3 at 10 GHz	Suitable as a driver amplifier in receiver/transmitter chains.
Good Directivity, 47.4 dB typ.	Isolates adjacent circuitry without need for an external expensive isolator.
Good input and output return loss	Eliminates need for external matching circuit providing published return loss.
Unpackaged Die	Enables the user to integrate the amplifier directly into hybrids

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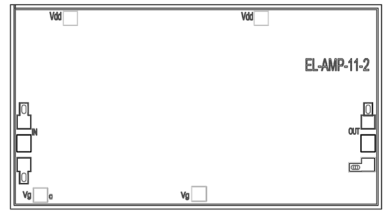

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- Good OIP3, 27.4 dBm at 10 GHz
- Good Directivity, 47.4 dBtyp.

Typical Applications
- Instrumentation
- Cellular Infrastructure
- Defense
- Test & Measurement

+RoHS Compliant
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Ordering Information: Refer to Last Page

General Description
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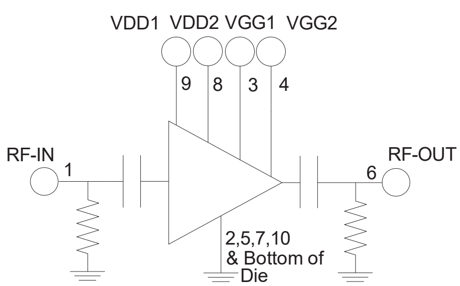
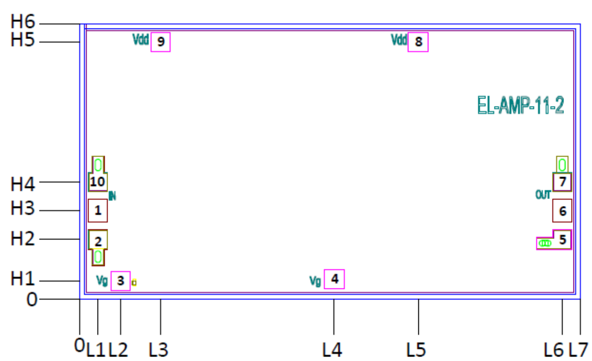
Simplified Schematic and Pad description



Pad #	Description
1	RF-IN
2,3,5,7 & Bottom of die	GROUND
3	VGG1
4	VGG2
6	RF-OUT
8	VDD2
9	VDD1

Bonding Pad Position



Dimensions in µm, Typical

L1	L2	L3	L4	L5	L6	L7	H1	H2	H3	H4	H5	H6
95	211	422	1328	1767	2519	2614	98	312	462	612	1343	1438

Thickness	Die size	Pad size 1 & 6	Pad size 2,3,5,7,8,9 & 10	Pad size 4
100	2614 x 1438	93 x 113	93 x 93	96 X 96

Electrical Specifications at 25°C, V_{DD}=4V, I_{DD}=210mA & Zo=50Ω unless noted

Parameter	Condition (MHz)	V_{DD}=4V[1] Min.	Typ.	Max.	Units
Frequency range[1]		2		18	GHz
Gain	2000		15.9		dB
	5000		16.1		
	10000		17.2		
	15000		16.7		
	18000		16.9		
Input return loss	2000		12		dB
	5000		16		
	10000		14		
	15000		11		
	18000		14		
Output return loss	2000		18		dB
	5000		20		
	10000		19		
	15000		16		
	18000		15		
Directivity	2000 - 18000		47.4		dB
Output power @1dB compression	2000		18.9		dBm
	5000		19.3		
	10000		19.6		
	15000		18.2		
	18000		17.6		
Output IP3 (Pout=0dBm/Tone)	2000		31.2		dBm
	5000		29.1		
	10000		27.4		
	15000		25.2		
	18000		23.7		
Noise figure	2000		6.8		dB
	5000		6.4		
	10000		5.5		
	15000		4.7		
	18000		5.1		
Device Operating Voltage (V_{DD})			4		V
Device Operating Current(I_{DD})			210		mA
Device Gate Voltage(V_{GG})			-0.46		V
Device Gate Current (I_{GG})			-0.2		μA
Thermal Resistance, Junction-to-ground lead			38.8		°C/W

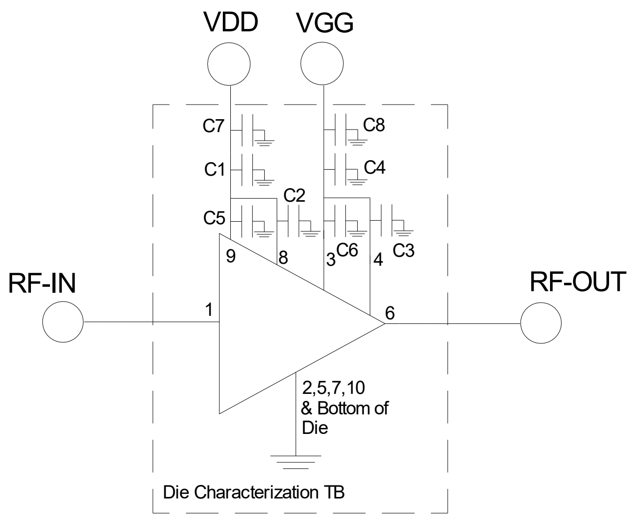
1. Die is tested in die characterization board. See characterization circuit (Fig. 1).

Absolute Maximum Ratings[2]

Parameter	Ratings
Operating Temperature (ground lead)	-40°C to +85°C
Junction Temperature	150°C
Power Dissipation	1.7W
Input Power (CW)	+23 dBm (5 minute max) +14 dBm (continuos)
DC voltage on RF-OUT & V_{DD}	7V
DC voltage on V_{GG}	-1.5V to -0.2V
Current I_{GG}	-5mA to 0mA
Current I_{DD}	320mA

2. Permanent damage may occur in any of these limits are exceeded.
Electrical maximum ratings are not intended for continuous normal operation.

Characterization & Characterization Test Circuit



Component	Value	Size	Part Number	Manufacturer
C2, C3, C5 & C6	100pF	22x22mil	MA4M3100	MACOM
C1 & C4	0.1uF	0402	GRM155R71A474KE01D	Murata
C7 & C8	10uF	1206	CL31B106KBHNNNE	Samsung

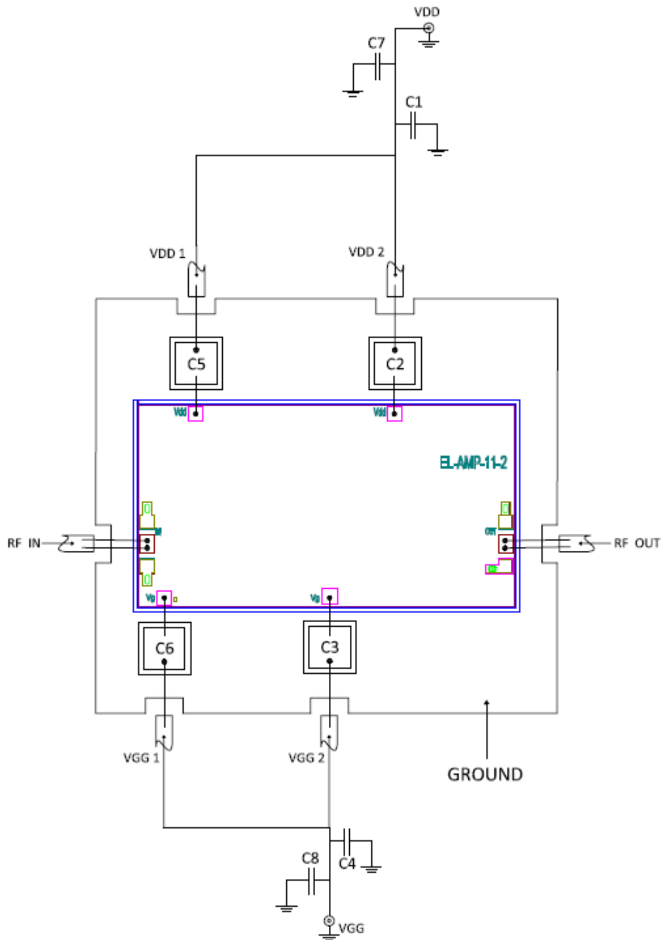
Fig 1. Characterization & Application Test Circuit
Note: This block diagram is used for characterization. (Die is attached and wire-bonded on die characterization test board. Gain, Return Loss, Output power at1dB compression (P1dB), output IP3 (OIP3) and noise figure are measured using Agilent's N5242A PNA-X microwave network analyzer.

Conditions:
1. VDD=4V
2. VG is set to obtain desired IDD as shown in specification table.3.Gain and Return loss: Pin= -25dBm
3. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 0 dBm/tone at output.

Power ON Sequence:
1) Turn on VGG =-1.3V
2) Turn on VDD = 4V
3) Adjust VGG until IDD=210mA (Typically, VGG = -0.46V)

Power OFF Sequence:
1) Turn back VGG = -1.3V
2) Turn off VDD
3) Turn off VGG

Assembly Diagram



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Assembly and Handling Procedure

1. Storage
   Dice should be stored in a dry nitrogen purged desiccators or equivalent.

2. ESD
   MMIC PHEMT amplifer dice are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic protected material, which should be open in clean room conditions at an appropriately grounded anti-static workstation.

3. Die Handling and Attachment
   Devices need careful handling using correctly designed collets, it is recommended to handle the chip along the edges with a custom design collet. The die mounting surface must be clean and flat. Using conductive silver filled epoxy, recommended epoxies are Ablestik 84-1 LMISR4 or equivalents. Apply sufficent epoxy to meet required epoxy bond line thickness, epoxy fillet height and epoxy coverage around total periphery. Parts shall be cured in a nitrogen filled atmosphere per manufacturer's cure condition. The surface of the chip has exposed air bridges and should not be touched with vacuum collet, tweezers or fingers.

4. Wire Bonding
   Bond pad openings in the surface passivation above the bond pads are provided to allow wire bonding to the dice gold bond pads. Thermo-sonic bonding is used with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. Suggested wire is pure gold, 1mil diameter. Bonds must be made from the bond pads on the die to the packaged or substrate. All bond wires should be kept as short as low as reasonable to minimize performance degradation due to undesirable series inductance.

Additional Detailed Technical Information *additional information is available on our dash board.*	
Performance Data	Data Table
	Swept Graphs
	S-Parameter (S2P Files) Data Set with and without port extension(.zip file)
Case Style	Die
Die Ordering and packaging information	Quantity, Package — Model No. Small, Gel - Pak: 5,10,50,100 KGD* — LTA-2183-DG+ Medium†, Partial wafer: KGD*<570 — LTA-2183-DP+ †*Available upon request contact sales representative* Refer to AN-60-067
Environmental Ratings	ENV80

*Known Good Dice ("KGD") means that the dice are taken from PCM good wafer and visually inspected in question have been subjected to Mini-Circuits while this is not definitive, it does help to provide a higher degree of confidence that dice are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

Additional Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

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