Wideband

Monolithic Amplifier Die

LTA-5R183-D+

50Ω 0.5 to 18 GHz

The Big Deal

- Super Wideband, 0.5 to 18 GHz
- Excellent Gain Flatness(±1.6 dB up to 18 GHz)
- Good Directivity, 18 dB typ.

Product Overview

The LTA-5R183-D+ is a super wideband amplifier amplifier die that operates over 0.5 to 18 GHz fabricated using PHEMT process. It delivers excellent gain flatness, good return loss, medium current with good P1dB and OIP3 across a wide bandwidth without the need of external matching network.

Key Features

Feature	Advantages
Super Wideband: 0.5 to 18 GHz	General purpose wideband amplifier is suitable for various applications including HF, VHF thru KU band.
Excellent gain flatness ± 1.6 dB up to 18 GHz	As a desirable characteristic of a wideband amplifier, excellent gain flatness allows amplification of a signal without changing the waveform in time domain.
Good Directivity, 18 dB typ.	Isolates adjacent circuitry without need for an external expensive isolator.
Good input and output return loss	Eliminates need for external matching circuit providing published return loss.
Unpackaged Die	Enables the user to integrate the amplifier directly into hybrids

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Typical Applications

- Instrumentation
- Cellular Infrastructure
- Defense

+RoHS Compliant

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Ordering Information: Refer to Last Page

General Description

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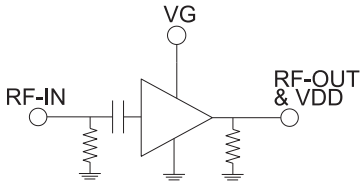
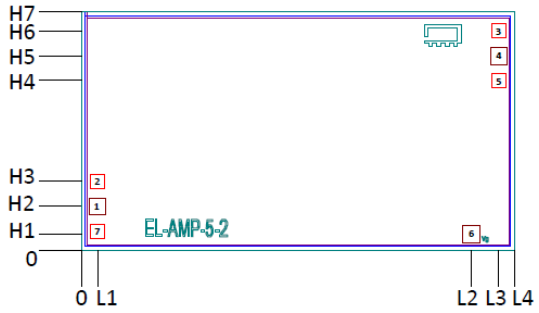
Simplified Schematic and Pad description



Pad #	Description
1	RF-IN
4	RF-OUT & VDD
6	VG
2,3,5,7 & Bottom of die	GROUND

Bonding Pad Position



Dimensions in µm, Typical

L1	L2	L3	L4	H1	H2	H3	H4	H5	H6	H7
96	2351	2518	2614	99	267	417	1024	1172	1324	1438

Thickness	Die size	Pad Size 1,4 & 6	Pad size 2,3,5,7
100	2614 x 1438	100 x 100	85 x 85

Electrical Specifications at 25°C, V_{DD}=5V, I_{DD}=85mA & Zo=50Ω unless noted

Parameter	Condition (MHz)	V_{DD}=5V[1] Min.	Typ.	Max.	Units
Frequency range[1]		0.5		18	GHz
Gain	500		14.6		dB
	5000		12.9		
	10000		13.3		
	15000		12.5		
	18000		13.1		
Input return loss	500		12		dB
	5000		12		
	10000		13		
	15000		9		
	18000		12		
Output return loss	500		36		dB
	5000		25		
	10000		34		
	15000		16		
	18000		17		
Reverse isolation	10000		38.4		dB
Output power @1dB compression	500		19.5		dBm
	5000		19.7		
	10000		18.6		
	15000		17.7		
	18000		16.3		
Output IP3[2]	500		31.3		dBm
	5000		27.4		
	10000		23.3		
	15000		21.7		
	18000		20		
Noise figure	500		4.8		dB
	5000		3.3		
	10000		2.8		
	15000		3.6		
	18000		4.4		
Device Operating Voltage (V_{DD})		4.75	5	5.25	V
Device Operating Current(I_{DD})			85		mA
Device Gate Voltage(V_G)			-0.94		V
Device Gate Current (I_G)			0.47		µA
Device Current Variation vs. Temperature[3]			264.5		µA/°C
Device Current Variation vs. Voltage[4]			0.007		mA/mV
Thermal Resistance, Junction-to-ground lead at 85°C stage temperature			22.2		°C/W

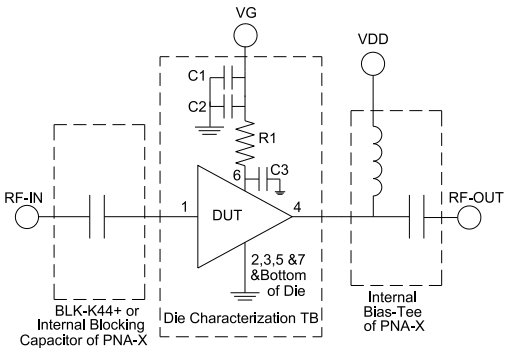
1. Die is tested in die characterization board. See characterization circuit (Fig. 1)
2. Tested at Pout=0dBm / tone.
3. Current variation over temperature=(Current at 100°C — Current at -55°C)/155°C
4. Current variation over voltage=(Current at 5.25V-current - Current at 4.75V)/1000

Absolute Maximum Ratings[5]

Parameter	Ratings
Operating Temperature (ground lead)	-55°C to 100°C
Junction Temperature	150°C
Power Dissipation	4.4W[6]
Input Power (CW)	+22 dBm
DC voltage on RF-OUT & V_{DD}	7V
DC voltage on V_G	-0.5V to -2V
DC voltage on RF-IN[7]	7V
Current I_{DD}	250mA
Current I_G	2mA

5. Permanent damage may occur in any of these limits are exceeded. Electrical maximum ratings are not intended for continuous normal operation.
6. Derates linearly 1.57W at 100°C.
7. DC signal at RF-IN will be blocked by internal blocking capacitor. However, a DC current of 3.5µA will be present due to the input shunt resistor assuming V_{RF-IN}=7V.

Characterization Test Circuit



Component	Size	Value	Part Number	Manufacturer
R1	0402	1K Ohm	FC0402E1001DTT5	Vishary
C1	0402	100pF	GRM1555C1H101JA01J	Murata
C2	0402	0.1uF	GRM155R71C104KA88D	Murata
C3	Chip Capacitor	100pF	MA4M3100	MACOM

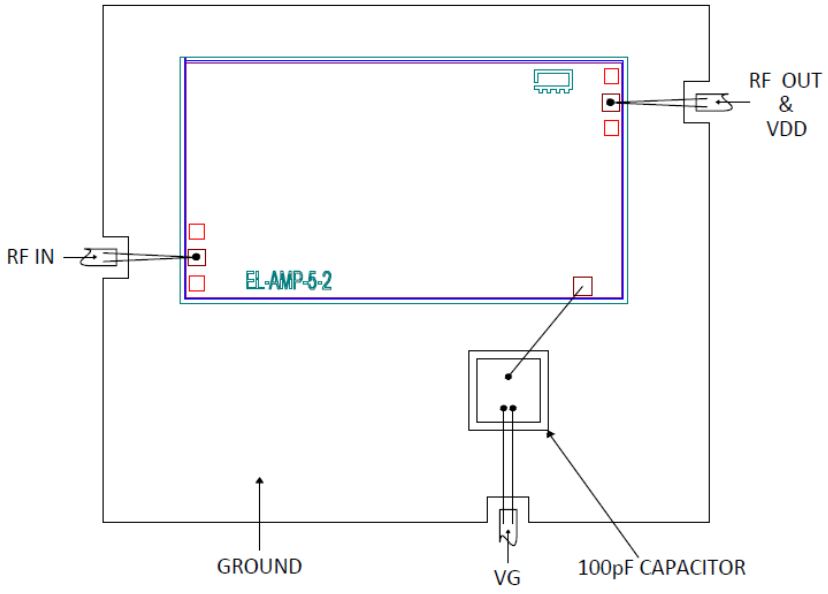
Fig 1. Characterization Circuit
Note: This block diagram is used for characterization. (Die is attached and wire-bonded on die characterization test board. Gain, Return loss, Output power at 1dB compression (P1dB), output IP3 (OIP3) and noise figure are measured using Agilent's N5242A PNA- X microwave network analyzer.

Conditions:
1. V_{DD}=5V
2. VG is set to obtain desired IDD as shown in specification table.
3. Gain and Return loss: Pin= -25dBm
4. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 0 dBm/tone at output.

Switch ON/OFF sequence:
1. To switch the amplifier ON:
   a. Turn on V_G with V_G=-1.1V
   b. Turn on V_{DD} with V_{DD}=5V
   c. Increase V_G to obtain desired I_{DD} as shown in specification table.
   d. Apply RF signal

2. To switch the amplifier OFF:
   a. Turn OFF RF signal
   b. Turn OFF V_{DD}
   c. Turn OFF V_G

Assembly Diagram



Assembly and Handling Procedure

1. Storage
   Dice should be stored in a dry nitrogen purged desiccators or equivalent.

2. ESD
   MMIC PHEMT amplifier dice are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic protected material, which should be open in clean room conditions at an appropriately grounded anti-static workstation.

3. Die Handling and Attachment
   Devices need careful handling using correctly designed collets, it is recommended to handle the chip along the edges with a custom design collet. The die mounting surface must be clean and flat. Using conductive silver filled epoxy, recommended epox ies are DieMat DM6030HK-PT/H579 or Ablestik 84-1 LMISR4 or equivalents. Apply sufficient epoxy to meet required epoxy bond line thickness, epoxy fillet height and epoxy coverage around total periphery. Parts shall be cured in a nitrogen filled atmosphere per manufacturer's cure condition. The surface of the chip has exposed air bridges and should not be touched with vacuum col let, tweezers or fingers.

4. Wire Bonding
   Bond pad openings in the surface passivation above the bond pads are provided to allow wire bonding to the dice gold bond pads. Thermo-sonic bonding is used with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. Suggested wire is pure gold, 1mil diameter. Bonds must be made from the bond pads on the die to the packaged or substrate. All bond wires should be kept as short as low as reasonable to minimize performance degradation due to undesirable series inductance.

Additional Detailed Technical Information

additional information is available on our dash board.

Performance Data	Data Table	
	Swept Graphs	
	S-Parameter (S2P Files) Data Set with and without port extension(.zip file)	
Case Style	Die	
Die Ordering and packaging information	Quantity, Package	Model No.
	Small, Gel - Pak: 5,10,50,100 KGD*	LTA-5R183-DG+
	Medium†, Partial wafer: KGD*<510	LTA-5R183-DP+
	Large†, Full Wafer	LTA-5R183-DF+
	†*Available upon request contact sales representative*	
	Refer to AN-60-067	
Environmental Ratings	ENV80	

*Known Good Dice ("KGD") means that the dice are taken from PCM good wafer and visually inspected in question have been subjected to Mini-Circuits while this is not definitive, it does help to provide a higher degree of confidence that dice are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

ESD Rating**

Human Body Model (HBM): Class 1A (pass 250V) in accordance with ANSI/ESD STM 5.1 - 2001

** Tested in 4.24x4.24mm, 10 Lead, LTCC package

Additional Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

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