Ultra Wideband, Flat Gain

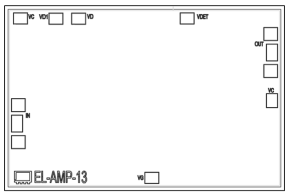
Monolithic Amplifier Die

LTA-M1109-D+

50Ω DC to 50 GHz

The Big Deal

- Ultra Wideband, DC to 50 GHz
- Excellent Gain Flatness, ±2.2 dB over 0.1 to 50 GHz
- May be used as a replacement model for MAAM-011109-DIE[a,b]



Product Overview

The LTA-M1109-D+ is an ultra-wideband distributed amplifier die that provides medium gain and excellent gain flatness over DC to 50GHz. It is fabricated using PHEMT process that delivers exceptional broadband RF performance. The amplifier has good P1dB and OIP3 performance. And it is also well-matched to 50Ω, requiring no external matching circuits to achieve published performance.

Key Features

Feature	Advantages
Ultra Wideband: DC to 50GHz	General purpose wideband amplifier is suitable for various applications
Medium Gain • 17.3 dB at 0.1GHz • 17.4 dB at 45 GHz	Minimizes the number of gain stages required to achieve published gain, reducing component count, cost and complexity.
Good P1dB • 20.7 dBm at 0.1GHz • 17.9 dBm at 30GHz	Useful as a driver amplifier. Can be used as a final amplifier in local oscillator chains to drive 17dBm mixers.
Unpackaged die	Enables user to integrate it directly into hybrids.

Notes:
a. Suitability for model replacement within a particular system must be determined by and is solely the responsibility of the customer based on, among other things, electrical performance criteria, stimulus conditions, application and compatibility with other components and environmental conditions and stresses.
b. The MAAM-011109-DIE part number is used for identification and comparison purposes only.

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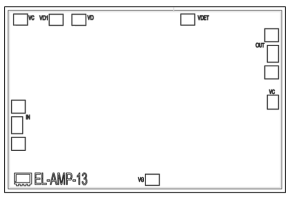


+RoHS Compliant
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Ordering Information: Refer to Last Page

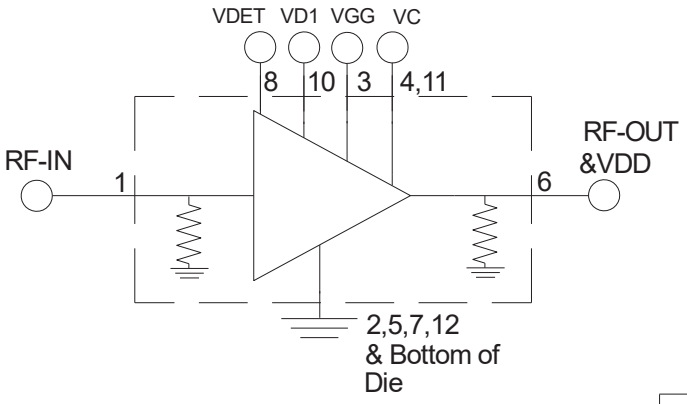
Typical Applications

- 5G
- Point-to-point Radio
- Military
- Instrumentation

General Description

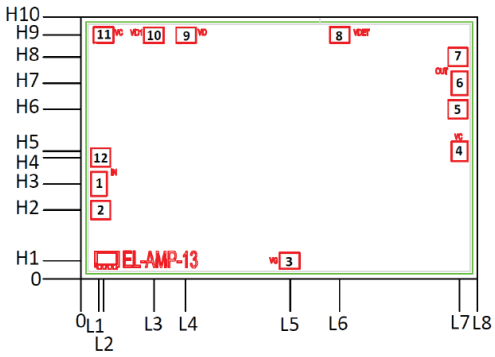
The LTA-M1109-D+ is an ultra-wideband distributed amplifier die that provides medium gain and excellent gain flatness over DC to 50GHz. It is fabricated using PHEMT process that delivers exceptional broadband RF performance. The amplifier has good P1dB and OIP3 performance. And it is also well-matched to 50Ω, requiring no external matching circuits to achieve published performance.

Simplified Schematic and Pad description



Pad #	Function	Description
1	RF-IN	RF Input Pad
3	VGG	Gate Bias Pad
4&11	VC	Gain Control Pads
6	RF-OUT & VDD	RF Output and Drain Pad
8	VDET	Voltage Detector Pad
9	VD	Alternative Drain Bias Pad, connects to Pad#6 internally.
10	VD1	Alternative Drain Bias Pad. It is terminated by C2
2,5,5,7 & Bottom of die	GROUND	Connects to ground

Bonding Pad Position



Dimensions in µm, Typical

L1	L2	L3	L4	L5	L6	L7	L8	H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
88	112	363	520	1040	1285	1882	1970	89	341	471	601	633	841	971	1101	1211	1300

Thickness	Die size	Pad size 1,6	Pad size 2,5,7,12	Pad size 3,8,9,10&11	Pad size 4
100	1970 x 1300	73 x 113	91 x 86	93 x 73	73 x 93

Electrical Specifications[1] at 25°C, VC=Open, Zo=50Ω at T_{AMB}=25°C

Parameter	Condition (MHz)	V_{DD} = 5V, I_{DD} = 160mA			Units
		Min.	Typ.	Max.	
Frequency Range		DC		50	GHz
Gain	100		17.3		dB
	10000		15.6		
	20000		16.1		
	30000		17.4		
	40000		17.4		
	50000		13		
Input Return Loss	100		12		dB
	10000		15		
	20000		17		
	30000		22		
	40000		12		
	50000		25		
Output Return Loss	100		27		dB
	10000		21		
	20000		16		
	30000		16		
	40000		14		
	50000		12		
Isolation	100-45000		36		dB
Output Power @1dB Compression	100		20.7		dBm
	10000		20.0		
	20000		19.3		
	30000		17.9		
	40000		17.0		
	50000		--		
Output IP3	100		32		dBm
Pout = 5dBm/Tone	10000		27.3		
	20000		26.9		
	30000		22.5		
	40000		20.8		
	50000		--		
Noise Figure	100		5.5		dB
	10000		3.1		
	20000		4.0		
	30000		5.5		
	40000		7.8		
	50000		11.8		
V_{DD}			5.0		V
V_{GG}			-0.76		V
I_{DD}			160.0		mA
I_{GG}			-0.24		mA
Thermal Resistance Junction to Ground Pad			17.8		degC/W

1. Measured on Mini-Circuits Die Test Board (MB-091). See Characterization TB (Fig.2)
Starting Frequency of the device is dependent on the input blocking capacitor value.

Absolute Maximum Ratings[2]

Parameter	Ratings
Operating Temperature	-40°C to 85°C
Junction Temperature	150°C
Total Power Dissipation	1.8W
Input Power (CW)	17dBm
Drain Voltage (V_{DD})	7.5V
Gate Voltage (V_{GG})	-1.6V to -0.5V
Drain Current (I_{DD})	240mA
Gate Current (I_{GG})	-5mA to 0mA
Control Voltage(V_C)	-1V to 1.2V

2. Permanent damage may occur if these limits are exceeding.
3. If Vc is open, the measured voltage is 1.33V
We can control the gain by over-writting the Vc. (See Figure 1).

Fig 1. Gain vs. Control Voltage (Vc)

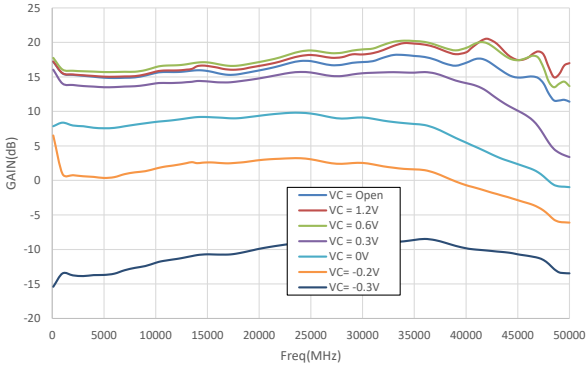
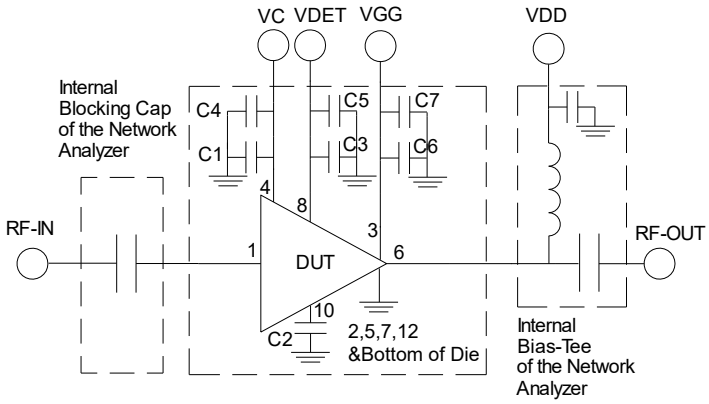


Fig. 2 Characterization & Application Test Circuit



Component	Value	Size	Part Number	Manufacturer
C1, C3 & C6	100pF	22 x 22mil	MA4M3100	MACOM Inc.
C2	820pF	20 x 20mil	SKT02C821M11A6	TECDIA Inc.
C4, C5 & C7	0.1uF	0402	GRM155R71C104KA88D	Murata

Fig 2. Assembly Drawing & Characterization Test Circuit
Note: This block diagram is used for characterization. Gain, Return loss, Output power at 1dB compression (P1dB), output IP3 (OIP3) and noise figure measured using Agilent's N5245B microwave network analyzer.

Conditions:
1. V_{DD} = 5V,
2. V_{GG} is set to obtain desired I_{DD} as shown in specification table.
3. Gain and Return loss: Pin= -25dBm
4. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, +5 dBm/tone at output.

Switch ON/OFF sequence:
1. To switch the amplifier ON:
a. Turn ON V_{GG} = -1.5V
b. Turn ON V_{DD} = 5V
c. Adjust V_{GG} to get I_{DD} = 160mA (Typically, VGG = -0.76V)

2. To switch the amplifier OFF:
a. Tune back V_{GG} = -1.5V
b. Turn OFF V_{DD}
c. Turn OFF V_{GG}

Fig. 3 Assembly Diagram

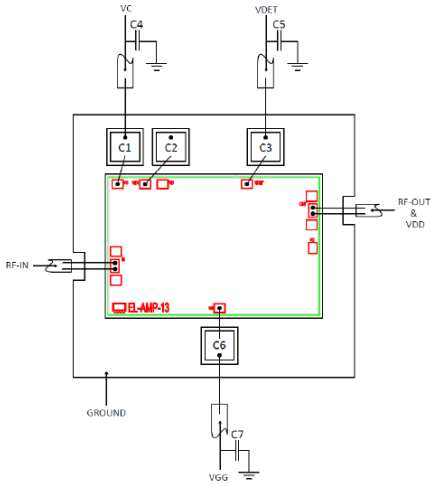
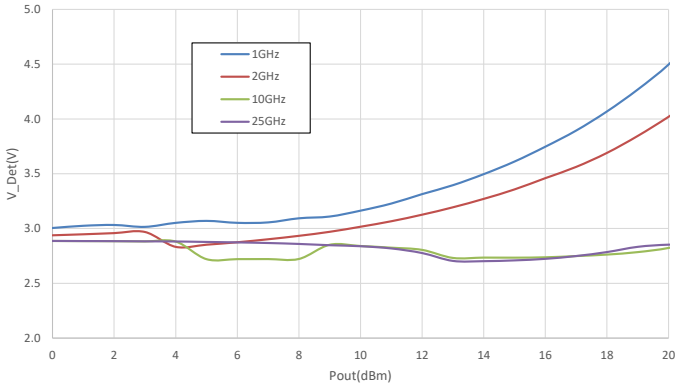


Fig. 4 Output Power vs. VDET



Assembly and Handling Procedure

1. Storage
   Dice should be stored in a dry nitrogen purged desiccators or equivalent.

2. ESD
   MMIC PHEMT amplifer dice are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic protected material, which should be open in clean room conditions at an appropriately grounded anti-static workstation.

3. Die Handling and Attachment
   Devices need careful handling using correctly designed collets, it is recommended to handle the chip along the edges with a custom design collet. The die mounting surface must be clean and flat. Using conductive silver filled epoxy, recommended epoxies are Ablestik 84-1 LMISR4 or equivalents. Apply sufficent epoxy to meet required epoxy bond line thickness, epoxy fillet height and epoxy coverage around total periphery. Parts shall be cured in a nitrogen filled atmosphere per manufacturer's cure condition. The surface of the chip has exposed air bridges and should not be touched with vacuum collet, tweezers or fingers.

5. Wire Bonding
   Bond pad openings in the surface passivation above the bond pads are provided to allow wire bonding to the dice gold bond pads. Thermo-sonic bonding is used with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. Suggested wire is pure gold, 1mil diameter. Bonds must be made from the bond pads on the die to the packaged or substrate. All bond wires should be kept as short as low as reasonable to minimize performance degradation due to undesirable series inductance.

Additional Detailed Technical Information

additional information is available on our dash board.

Performance Data	Data Table	
	Swept Graphs	
	S-Parameter (S2P Files) Data Set with and without port extension(.zip file)	
Case Style	Die	
Die Ordering and packaging information	Quantity, Package	Model No.
	Small, Gel - Pak: 5,10,50,100 KGD*	LTA-M1109-DG+
	Medium†, Partial wafer: KGD*<768	LTA-M1109-DP+
	†*Available upon request contact sales representative*	
	Refer to AN-60-067	
Environmental Ratings	ENV80	

*Known Good Dice ("KGD") means that the dice in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such dice fall within a predefined range. While DC testing is not definitive, it does help to provide a higher degree of confidence that dice are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

Additional Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.

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