MMIC DIE

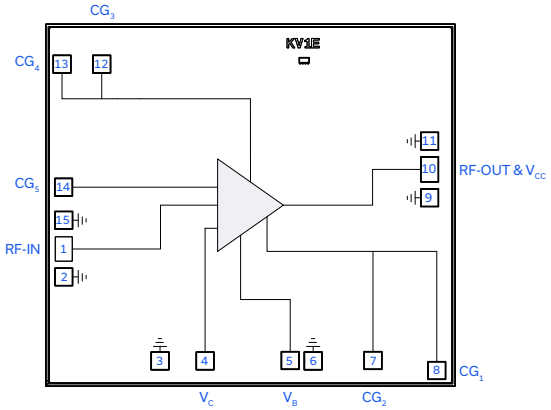
# Wideband Amplifier LVA-273PN-D+

50Ω 0.01 to 26.5GHz Ultra-Low Phase Noise

## THE BIG DEAL

- Wide Bandwidth 0.01 to 26.5 GHz
- Ultra-low Phase Noise Typ. -172 dBc/Hz @ 10 kHz Offset
- Output P1dB Typ. +18 dBm
- Output IP3 Typ. +28 dBm
- Supply Voltage: +5 V and 85 mA

## FUNCTIONAL DIAGRAM




SEE ORDERING INFORMATION ON THE LAST PAGE

## APPLICATIONS

- Test and Measurement Equipment
- Radar, EW, and ECM Defense Systems
- 5G MIMO and Back Haul Radio Systems
- Signal Distribution Networks

## PRODUCT OVERVIEW

Mini-Circuits LVA-273PN-D+ is an ultra-low phase noise distributed MMIC amplifier die fabricated on a GaAs HBT process technology. Operating from 0.01 to 26.5GHz, this amplifier features high dynamic range and ultra-low phase noise along with 18dB gain, +18 dBm P1dB, +28 dBm OIP3, and 3.7 dB noise figure. The LVA-273PN-D+ is ideal for use with low noise signal sources and highly sensitive transceiver signal chains for commercial, industrial, and defense applications.

## KEY FEATURES

| Features | Advantages |
|---|---|
| Wide Bandwidth: 0.01 to 26.5 GHz | Supports a broad variety of applications including Test and Measurement Equipment, 5G Microwave Radio, Radar, and Electronic Warfare Systems. |
| Ultra-low Phase Noise: -172 dBc/Hz @ 10kHz offset | Enables the detection of signal levels in the presence of noise. |
| High Dynamic Range:<br>• +18 dBm P1dB<br>• 18 dB Gain<br>• 3.7 dB Noise Figure | The MMIC amplifier's unique combinations of ultra-low phase noise, high operating P1dB, high Gain, and low noise figure features enable optimum performance for high dynamic range transceiver systems. |

REV. A
ECO-028392
LVA-273PN-D+
MCL NY
260206

# Wideband Amplifier LVA-273PN-D+

50Ω 0.01 to 26.5GHz Ultra-Low Phase Noise

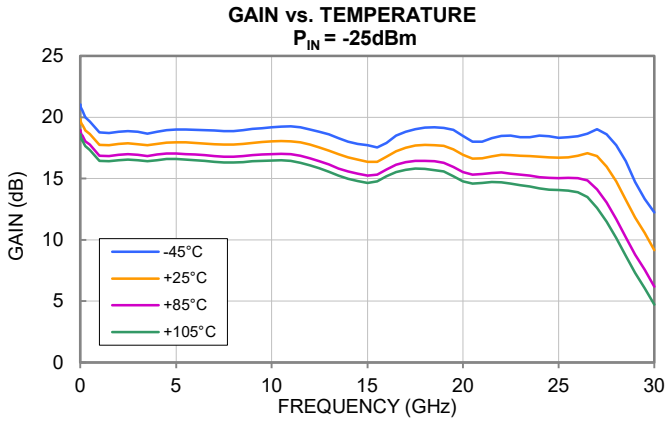
## ELECTRICAL SPECIFICATIONS[1] AT +25°C, $V_{CC}$ = +5 V, $V_C$ = +5 V, $V_B$ = +5 V, & Zo = 50Ω UNLESS NOTED OTHERWISE

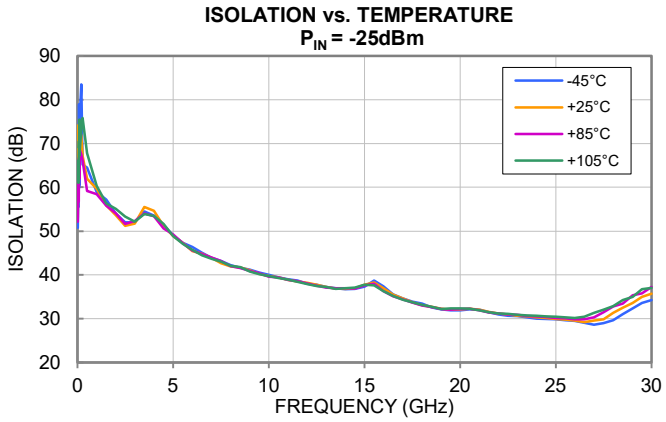
| Parameter | Condition (GHz) | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Frequency Range | | 0.01 | | 26.5 | GHz |
| Gain | 0.01 | | 19.9 | | dB |
| | 5 | | 18.0 | | |
| | 10 | | 18.0 | | |
| | 20 | | 16.9 | | |
| | 26.5 | | 17.3 | | |
| Input Return Loss | 0.01 | | 16.6 | | dB |
| | 5 | | 13.3 | | |
| | 10 | | 20.0 | | |
| | 20 | | 13.0 | | |
| | 26.5 | | 20.0 | | |
| Output Return Loss | 0.01 | | 17.9 | | dB |
| | 5 | | 15.5 | | |
| | 10 | | 19.6 | | |
| | 20 | | 13.0 | | |
| | 26.5 | | 20.0 | | |
| Isolation | 0.01-26.5 | | 41.0 | | dB |
| Output Power at 1dB Compression (P1dB)[2] | 0.01 | | +20.0 | | dBm |
| | 5 | | +18.1 | | |
| | 10 | | +18.5 | | |
| | 20 | | +15.7 | | |
| | 26.5 | | +11.9 | | |
| Output Power at 3dB Compression (P3dB)[3] | 0.01 | | +21.8 | | dBm |
| | 5 | | +21.2 | | |
| | 10 | | +20.6 | | |
| | 20 | | +17.2 | | |
| | 26.5 | | +14.4 | | |
| Output Third-Order Intercept Point ($P_{OUT}$ = -2dBm/Tone) | 0.01 | | +28.1 | | dBm |
| | 5 | | +26.8 | | |
| | 10 | | +27.7 | | |
| | 20 | | +25.4 | | |
| | 26.5 | | +18.1 | | |
| Input Third-Order Intercept Point ($P_{OUT}$ = -2dBm/Tone) | 0.01 | | +8.2 | | dBm |
| | 5 | | +8.8 | | |
| | 10 | | +9.7 | | |
| | 20 | | +8.5 | | |
| | 26.5 | | +0.8 | | |
| Noise Figure | 2 | | 7.6 | | dB |
| | 5 | | 4.3 | | |
| | 10 | | 3.6 | | |
| | 20 | | 5.5 | | |
| | 26.5 | | 7.9 | | |
| Additive Phase Noise (@10kHz Offset) | | | -172 | | dBc/Hz |
| Device Operating Voltage ($V_{CC}$) | | +4.75 | +5 | +5.25 | V |
| Device Operating Current ($I_{CC}$)[4] | | | 85 | | mA |
| Control Voltage ($V_C$) | | | +5 | | V |
| Control Current ($I_C$) | | | 1.2 | | mA |
| Base Voltage ($V_B$) | | | +5 | | V |
| Base Current ($I_B$) | | | 4.5 | | mA |
| Device Current Variation vs. Temperature[5] | | | 7 | | uA/°C |
| Device Current Variation vs. Voltage[6] | | | 0.013 | | mA/mV |

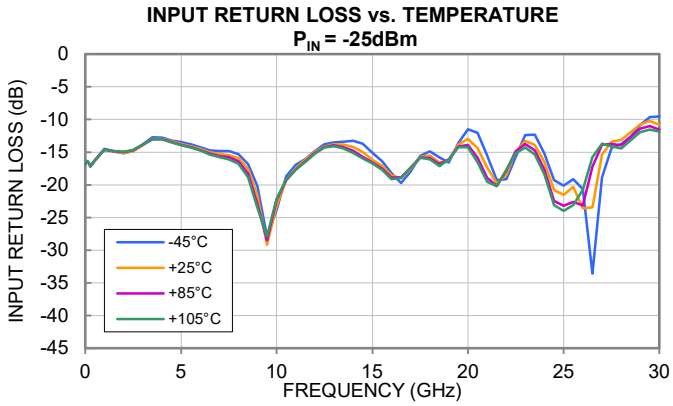
1. Tested on Mini-Circuits Die Characterization Test Board. See Figure 2. De-embedded to the device reference plane. Device does not feature internal blocking capacitors so that low frequency performance could be achieved.
2. Defined as Output Power at which Gain is compressed by 1dB.
3. Defined as Output Power at which Gain is compressed by 3dB.
4. Current at $P_{IN}$= -25dBm. Increases to 105mA at P3dB
5. ((Current in mA at +105°C) - (Current in mA at -45°C)) / (+150°C)
6. ((Current in mA at +5.25V) - (Current in mA at +4.75V )) / ((+5.25V - +4.75V) * 1000mA/mV)

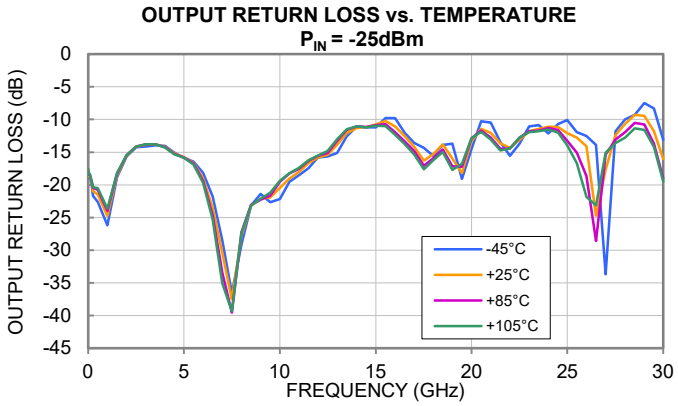
## TYPICAL PERFORMANCE GRAPHS

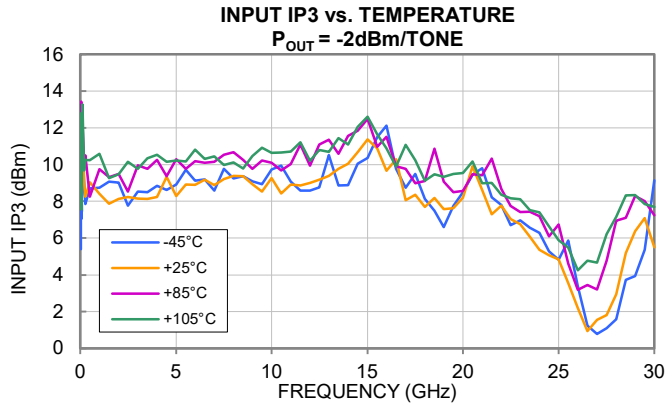
Note: All data taken at nominal conditions $V_{CC}$ = +5V, $V_C$ = +5V, and $V_B$ = +5V unless noted otherwise.

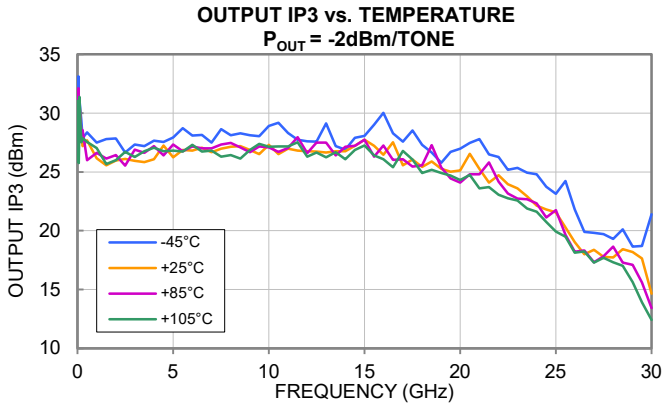


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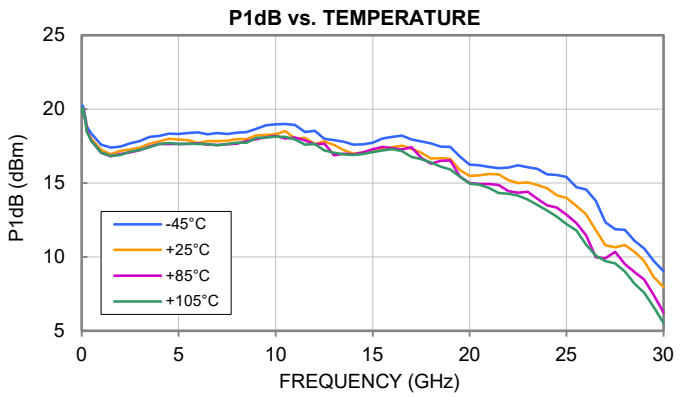
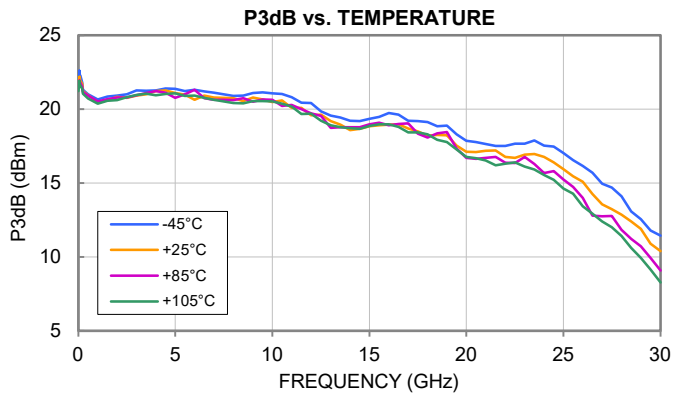
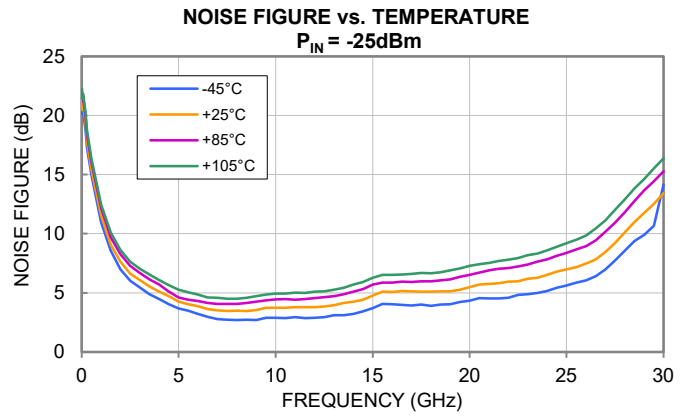
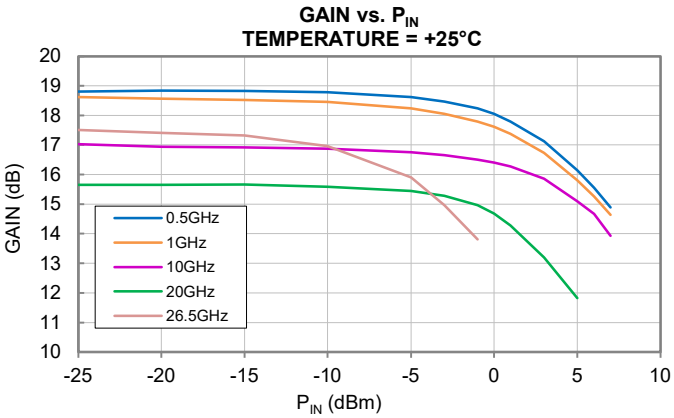
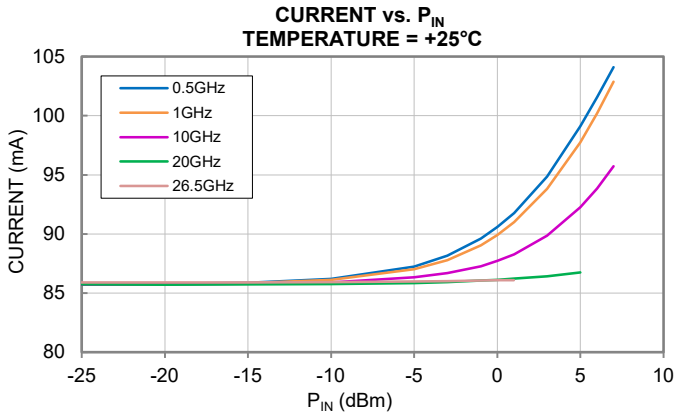
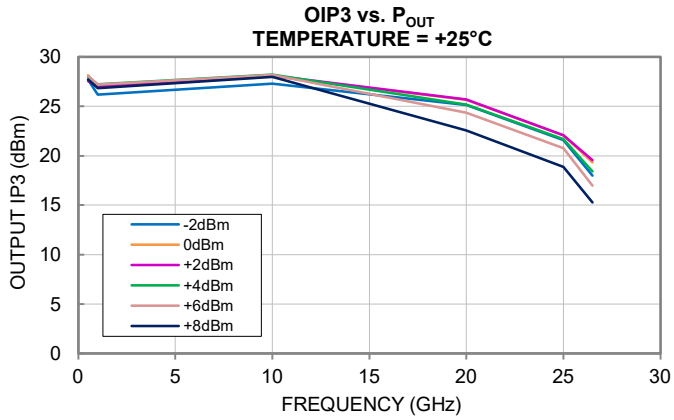


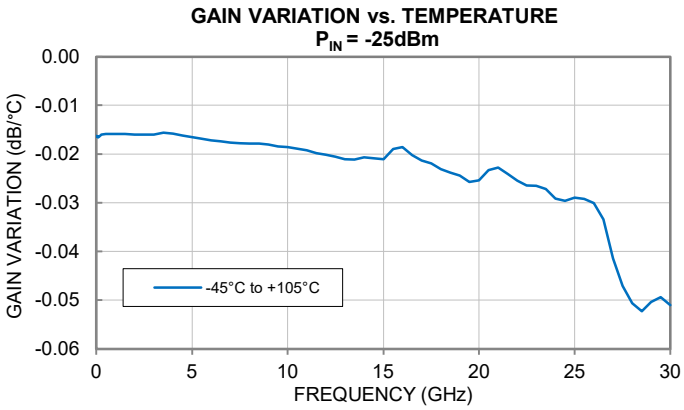



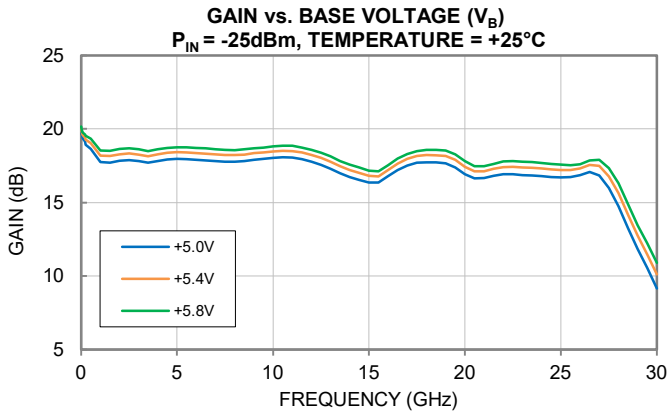



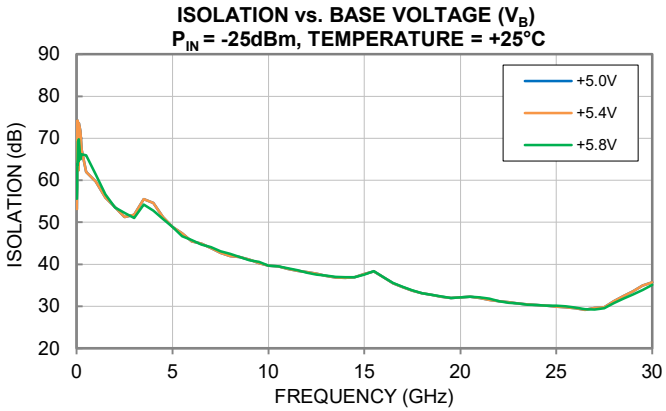



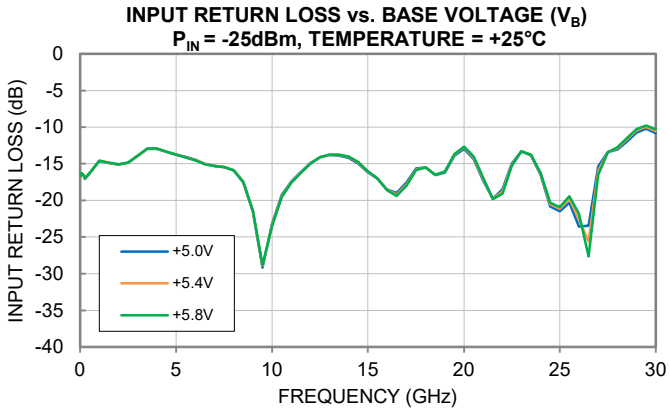
## TYPICAL PERFORMANCE GRAPHS

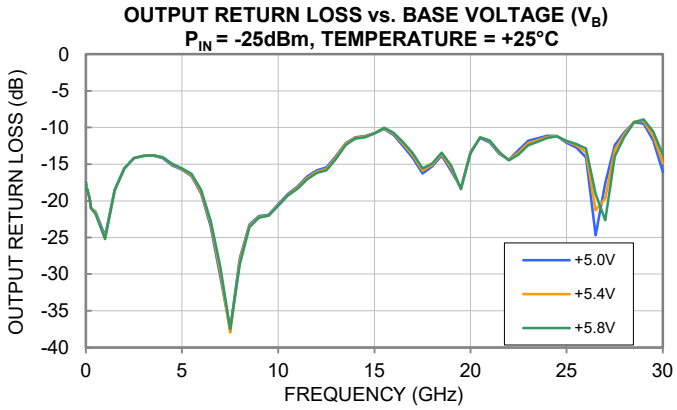
Note: All data taken at nominal conditions $V_{CC}$ = +5V, $V_C$ = +5V, and $V_B$ = +5V unless noted otherwise.

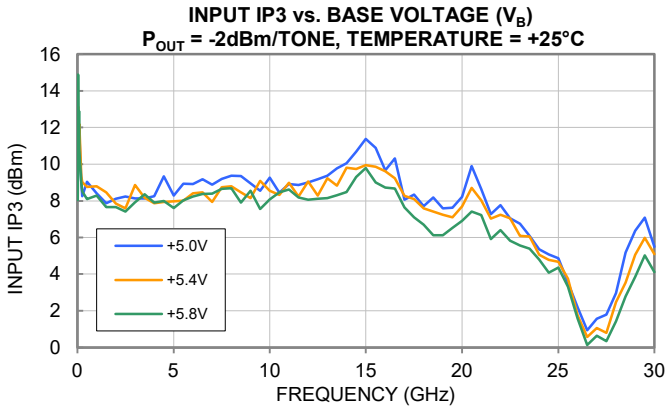


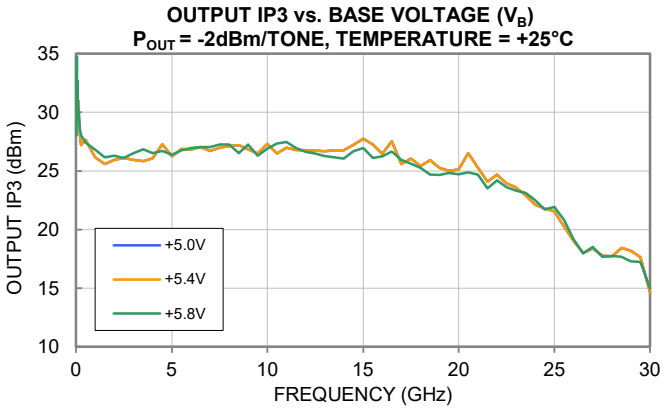



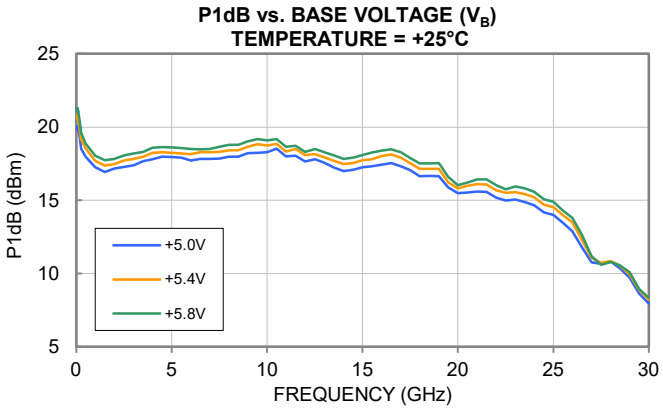



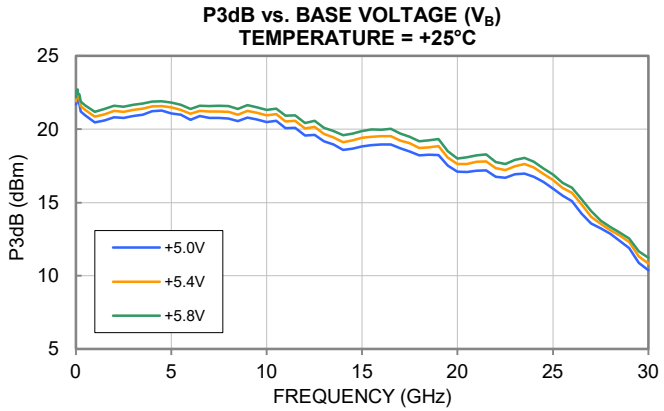



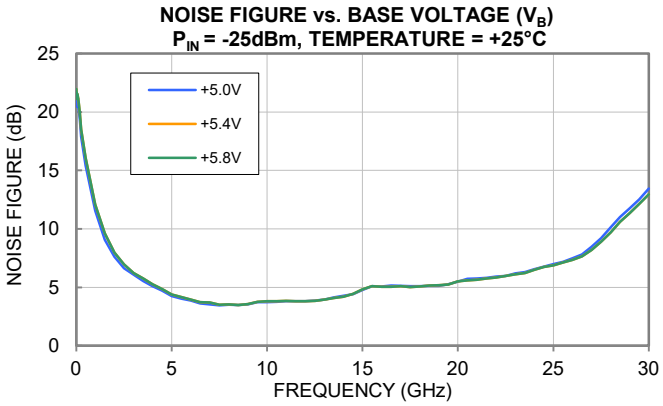
## TYPICAL PERFORMANCE GRAPHS

Note: All data taken at nominal conditions $V_{CC}$ = +5V and $V_C$ = +5V unless noted otherwise.



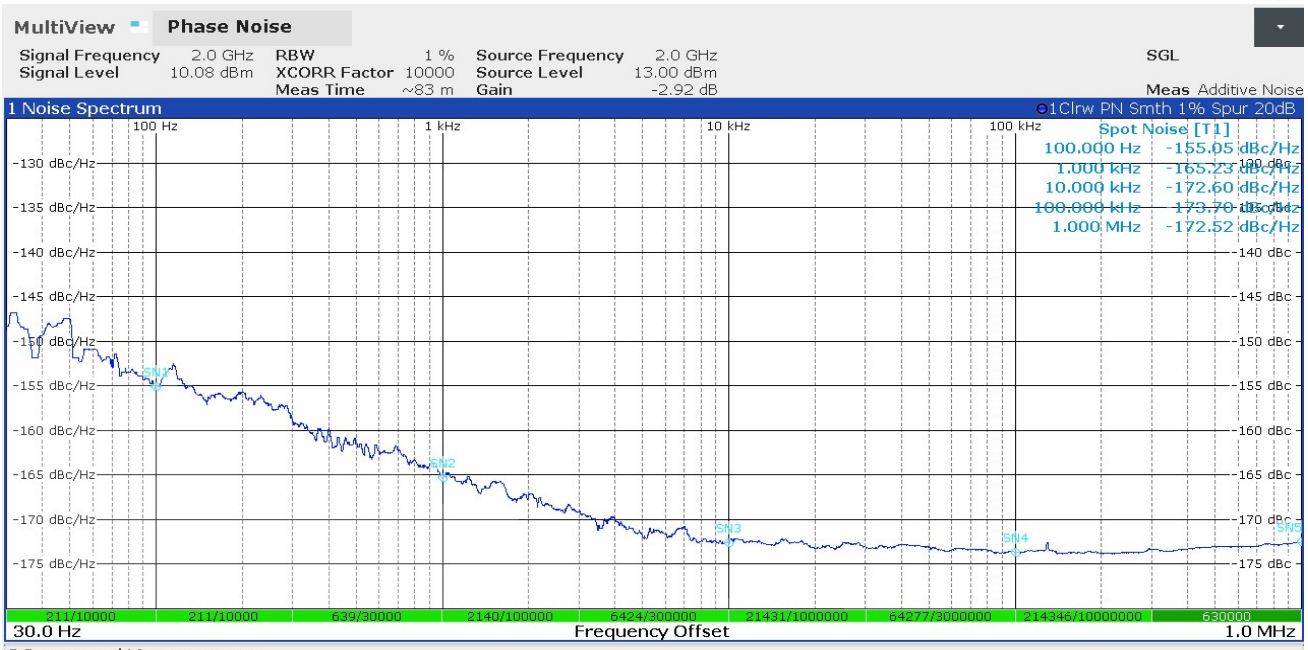



## TYPICAL PERFORMANCE GRAPHS

Note: All data taken at nominal conditions $V_{CC}$ = +5V, $V_C$ = +5V, and $V_B$ = +5V unless noted otherwise.




Note: Tested in a 4x4mm 24-lead QFN-style package.

## ABSOLUTE MAXIMUM RATINGS[7]

| Parameter | Ratings |
|---|---|
| Operating Temperature (ground lead)[8] | -45°C to +105°C |
| Storage Temperature[9] | +20°C to +35°C |
| Total Power Dissipation | 1.54 W |
| Junction Temperature[10] | +150 °C |
| Input Power (CW), $V_{CC}$ = +5 V, $V_C$ = +5 V, $V_B$ = +5 V | +25 dBm |
| DC Voltage on RF-OUT & $V_{CC}$ | +10 V |
| DC Voltage on RF-IN | +10 V |
| Current $I_{CC}$ | 150 mA |
| DC Voltage on $V_C$ | +10 V |
| Current $I_C$ | 5 mA |
| DC Voltage on $V_B$ | +10 V |
| Current $I_B$ | 14 mA |

7. Permanent damage may occur if any of these limits are exceeded. Maximum ratings are not intended for continuous normal operation.
8. Bottom of Die.
9. For die shipped in Gel-Pak see ENV80 (limited by packaging)
10. Peak temperature on top of Die.

## THERMAL RESISTANCE

| Parameter | Ratings |
|---|---|
| Thermal Resistance ($\Theta_{jc}$)[11] | 29.2 °C/W |

11. $\Theta_{jc}$= (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

## ESD RATING[12]

| | Class | Voltage Range | Reference Standard |
|---|---|---|---|
| HBM | 1B | 500V to < 1000V | ANSI/ESDA/JEDEC JS-001-2017 |
| CDM | C2 | 500V to < 1000V | JESD22-C101F |

ESD HANDLING PRECAUTION: This device is designed to be Class 1B for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage.

12. Tested in 4x4mm 24-lead QFN-style package.

# Wideband Amplifier LVA-273PN-D+

50Ω 0.01 to 26.5GHz Ultra-Low Phase Noise

## FUNCTIONAL DIAGRAM

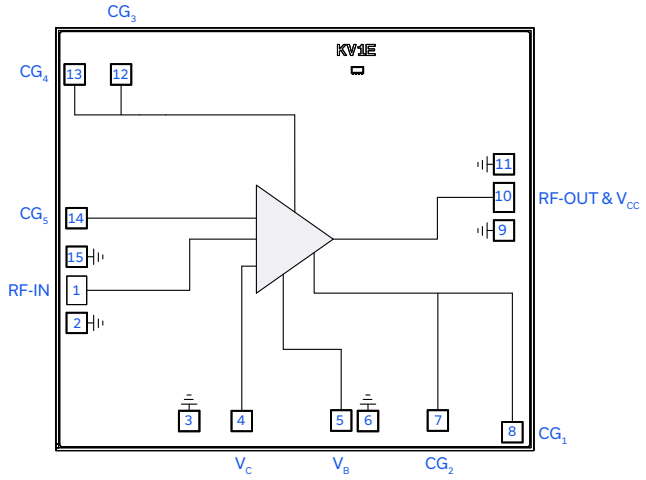
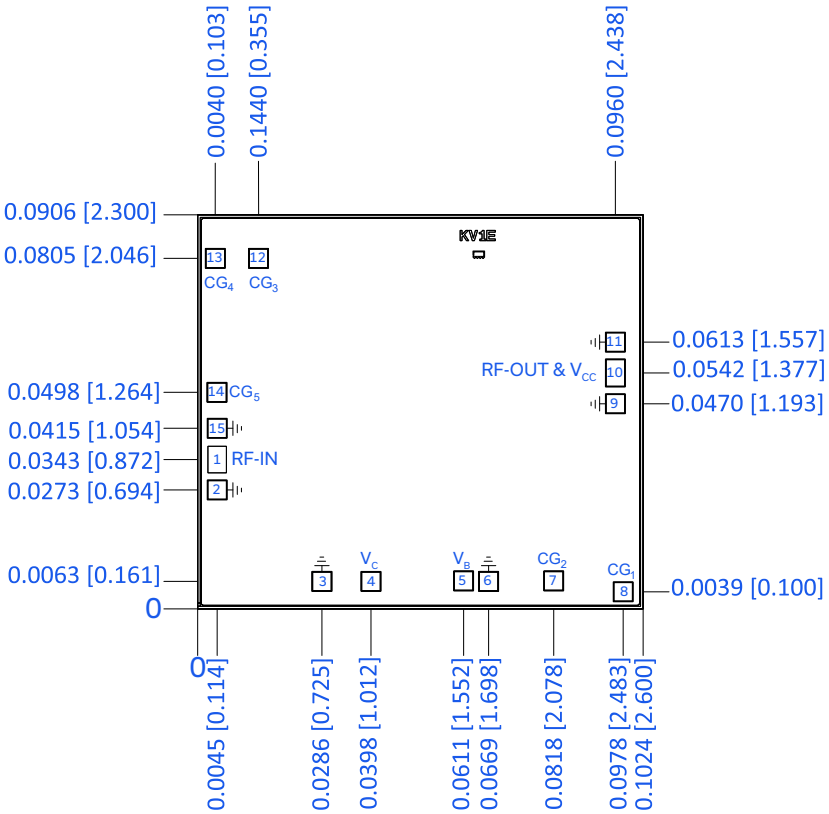



Figure 1. LVA-273PN-D+ Functional Diagram

## PAD DESCRIPTION

| Function | Pad # | Application Description (Refer to Figure 2) |
|---|---|---|
| RF-IN | 1 | RF-IN Pad connects to RF-Input port. |
| RF-OUT & $V_{CC}$ | 10 | RF-OUT Pad connects to RF-Output and $V_{CC}$ port. |
| $V_C$ | 4 | DC Input Pad connects to voltage input port, $V_C$. |
| $V_B$ | 5 | DC Input Pad connects to voltage input port, $V_B$. |
| $CG_1$ | 8 | Connects to AC ground through external capacitor C9. |
| $CG_2$ | 7 | Connects to AC ground through external capacitor C8. |
| $CG_3$ | 12 | Connects to AC ground through external capacitor C3. |
| $CG_4$ | 13 | Connects to AC ground through external capacitor C2. |
| $CG_5$ | 14 | Connects to AC ground through external capacitor C1. |
| GND | 2, 3, 6, 9, 11, 15, & Bottom of Die | Connects to ground. |

## DIE OUTLINE: inches [mm], Typical




## DIMENSIONS: inches [mm], Typical

| | |
|---|---|
| **Die Size** | 0.1024 x 0.0906 [2.600 x 2.300] |
| **Die Thickness** | 0.0040 [0.100] |
| **Bond Pad Sizes:** | |
| **Pad 1 & 10** | 0.0061 x 0.0061 [0.155 x 0.155] |
| **Pads 2-9, 11-15** | 0.0043 x 0.0043 [0.108 x 0.108] |
| **Plating (Pads & Bottom of Die)** | Gold |

## CHARACTERIZATION TEST BOARD

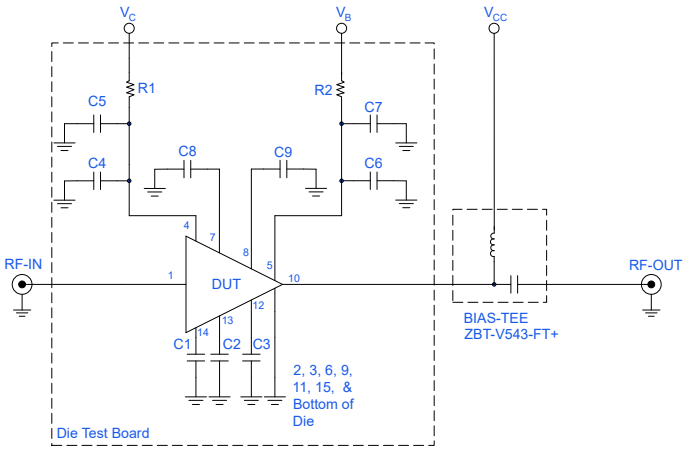



**Figure 2. Die Evaluation Board**

**Electrical Parameters and Conditions**
Gain, Return Loss, Output Power at 1dB Compression (P1dB), Output Power at 3dB Compression (P3dB), Output IP3 (OIP3), and Noise Figure measured using N5247B PNA-X Microwave Network Analyzer.

Conditions:
1. Gain, Noise Figure, and Return Loss: $P_{IN}$= -25dBm
2. Output IP3 (OIP3): Two tones, spaced 1MHz apart, -2dBm/tone at output.

Power On/Power Off Sequence
Caution: Permanent damage to the device will occur if the Power ON and Power OFF Sequences are not followed.

Power On:
1) Set $V_{CC}$ = +5V.
2) Set $V_C$ = +5V.
3) Set $V_B$ = +5V.
4) Turn on $V_{CC}$, $V_C$, and $V_B$.
5) Apply RF Signal.

Power Off:
1) Turn off RF Signal.
2) Turn off $V_{CC}$, $V_C$, and $V_B$.

Note: Mini-Circuits Bias Tee ZBT-V543-FT+ is external to the Characterization and Application Circuit. To achieve proper low frequency performance, no blocking capacitors were used on the input of the DUT.

| Component | Value | Size | Part Number | Manufacturer |
|---|---|---|---|---|
| C1 | 5100pF | 0603 | GCM1885C1H512JA16D | Murata |
| C2 | 1µF | 0603 | GCM188R71E105KA64J | Murata |
| C3, C9 | 1000pF | 0402 | GRM1555C1H102JA01D | Murata |
| C4, C6 | 100pF | 0402 | GRM1555C1H101JA01D | Murata |
| C5, C7, C8 | 0.1µF | 0402 | GRM155R71H104KE14J | Murata |
| R1, R2 | 0Ω | 0402 | RK73Z1ETTP | KOA Speer |

## ASSEMBLY DIAGRAM

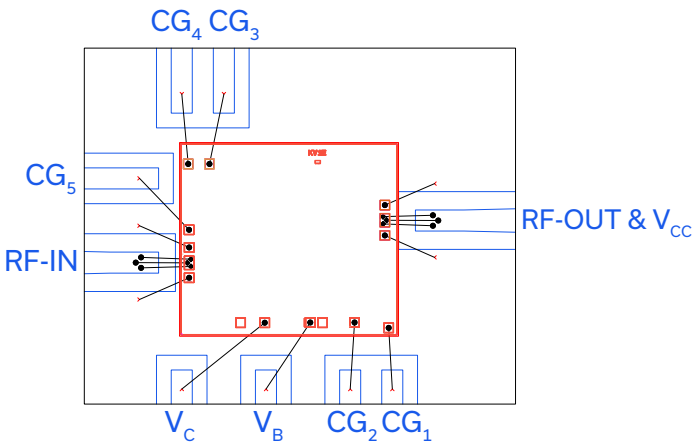



**Figure 3. LVA-273PN-D+ Assembly Diagram**

Refer to the table in Figure 2 for more details on the passive components.

- Bond wire diameter: 1mil
- Bond wire lengths from Die Pad to PCB at RF-IN & RF-OUT ports: 24 ± 2mils
- Typical Gap from Die edge to PCB edge: 3mils
- PCB thickness and material: 6.6mil RO4350B (Thickness : 1oz copper on each side).

## ASSEMBLY AND HANDLING PROCEDURE

1. Storage
   Die should be stored in a dry nitrogen purged desiccator or equivalent.
2. ESD Precautions
   MMIC pHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in anti-static protected material, which should be opened only in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
   Devices require careful handling using tools appropriate for manipulating semiconductor chips. It is recommended to handle the chips along the edges with a custom designed collet. The surface of the chips have exposed air bridges and should not be touched with a vacuum collet, tweezers or fingers. The die mounting surface must be clean and flat. Using conductive silver-filled epoxy, apply sufficient adhesive to meet the required bond line thickness, fillet height and coverage around the total periphery of the device. The recommended epoxy is Atrox 800HT5 Sintering or equivalent. Parts should be cured in a nitrogen-filled atmosphere per manufacturer's recommended cure profile.
4. Wire Bonding
   Openings in the surface passivation above the gold bond pads are provided to allow wire bonding to the die. Thermosonic bonding is recommended with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. The suggested interconnect is pure gold, 1 mil diameter wire. Bonds are recommended to be made from the bond pads on the die to the package or substrate. All bond wire length and bond wire height should be kept as short as possible, unless specified by design, to minimize performance degradation due to undesirable series inductance.

## ADDITIONAL DETAILED INFORMATION IS AVAILABLE ON OUR DASH BOARD CLICK HERE

| | | |
|---|---|---|
| **Performance Data** | Table<br>Graphs<br>S-Parameter (S2P Files) Data Set (.zip file) | |
| **Case Style** | Die | |
| **RoHS Status** | Compliant | |
| **Die Ordering and Packaging Information** | Quantity, Package | Model No. |
| | Gel - Pak: 5, 10, 50, KGD* | LVA-273PN-DG+ |
| | Medium†, Partial wafer: KGD*<399 | LVA-273PN-DP+ |
| | Full wafer† | LVA-273PN-DF+ |
| | †Available upon request contact sales representative. Refer to AN-60-067 | |
| **Die Marking** | KV1E | |
| **Environmental Ratings** | ENV80 | |

* Known Good Die ("KGD") means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within a predefined range. While DC testing is not definitive, it does provide a higher degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuits' applicable established test performance criteria and measurement instructions.

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E. Purchasers of this part are solely responsible for proper storing, handling, assembly and processing of known good die (KGD) (including, without limitation, proper ESD preventative measures, die preparation, die attach, wire bonding and related assembly and test activities), and Mini-Circuits assumes no responsibility therefor or for environmental effects on KGD.

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