MMIC DIE

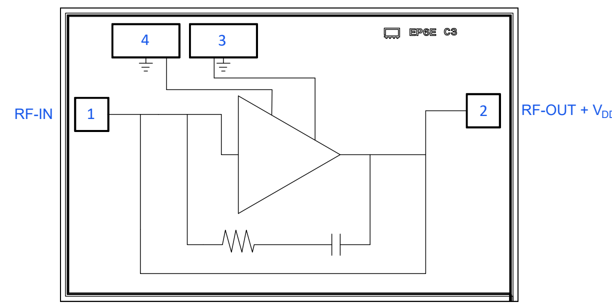
CATV Amplifier

PGA-32-75-D+

75Ω 5 to 300 MHz High Dynamic Range

THE BIG DEAL
- High OIP3, Typ. +43.3 dBm
- High P1dB, Typ. + 23.7 dBm
- High Gain, Typ. 15.6 dB
- Excellent Return Loss, Typ. 20 dB
- Single Supply Voltage, +5 V or +9 V

FUNCTIONAL DIAGRAM



SEE ORDERING INFORMATION ON THE LAST PAGE

APPLICATIONS
- CATV
- DOCSIS 3.1
- DOCSIS 4.0
- WLAN

PRODUCT OVERVIEW
Mini-Circuits' PGA-32-75-D+ is an amplifier die operating from 5 to 300 MHz that is fabricated using E-pHEMT technology, offering extremely high dynamic range with low noise figure, flat gain, and repeatable lot-to-lot performance. This amplifier boasts a high OIP3 of +43.3 dBm and a P1dB of +23.7 dBm, providing excellent linearity making it perfect for numerous CATV applications.

KEY FEATURES

Features	Advantages
Broadband: 5 to 300 MHz	5 to 300 MHz bandwidth covers primary CATV applications such as DOCSIS 3.1 & DOCSIS 4.0.
High IP3 Versus DC Power Consumption: Typ. +43.3 dBm	The PGA-32-75-D+ using E-pHEMT technology provides high IP3 performance relative to device size and power consumption.
High IP2: Typ. +57.2 dBm	Suppresses second order products on wideband applications such as CATV.
Unpackaged Die	Suitable for chip and wire hybrid assemblies.

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75Ω 5 to 300 MHz High Dynamic Range

ELECTRICAL SPECIFICATIONS[1] AT +25°C, Zo = 75Ω UNLESS NOTED OTHERWISE

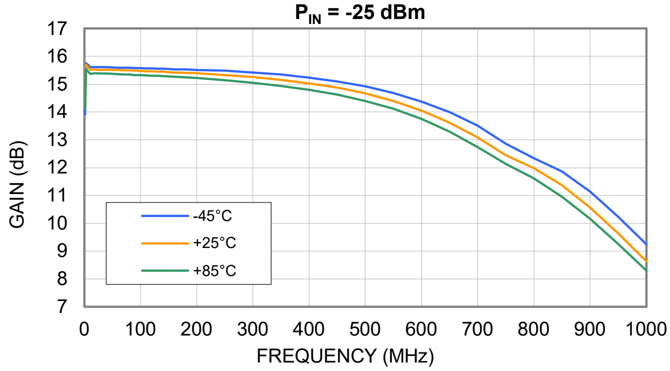
Parameter	Condition (MHz)	V_{DD} = +9 V			V_{DD} = +5 V	Units
		Min.	Typ.	Max.	Typ.	
Frequency Range		5		300		MHz
Gain	5		15.8		15.1	dB
	10		15.7		15.1	
	100	14.0	15.6	17.2	15.1	
	150		15.6		15.0	
	200		15.5		14.9	
	300		15.4		14.9	
Gain Flatness	5-300		±0.2		±0.3	dB
Input Return Loss	5		14		13	dB
	10		18		17	
	100		20		19	
	150		20		19	
	200		20		18	
	300		20		18	
Output Return Loss	5		20		19	dB
	10		20		20	
	100		20		20	
	150		20		20	
	200		20		20	
	300		19		20	
Isolation	5-300		20.6		20.3	dB
Output Power at 1 dB Compression (Total Composite Power)[2]	5		+20.4 (+69.1)		+18.1 (+66.8)	dBm (dBmV)
	10		+21.7 (+70.4)		+18.0 (+66.7)	
	100		+23.7 (+72.4)		+18.0 (+66.7)	
	150		+23.7 (+72.4)		+17.9 (+66.6)	
	200		+23.7 (+72.4)		+17.8 (+66.5)	
	300		+23.6 (+72.3)		+17.6 (+66.3)	
Output Third-Order Intercept (P_{OUT} = +5 dBm/Tone)	5		+43.2		+29.2	dBm
	10		+43.9		+31.1	
	100		+43.3		+31.6	
	150		+43.7		+32.3	
	200		+43.8		+32.6	
	300		+43.8		+32.9	
Output Second-Order Intercept (P_{OUT} = +5 dBm/Tone)	5		+57.3		+40.2	dBm
	10		+58.1		+40.9	
	100		+57.2		+41.5	
	150		+56.3		+41.5	
	200		+55.7		+41.5	
	300		+56.1		+42.2	
Noise Figure	5		-		-	dB
	10		3.8		3.8	
	100		2.9		2.6	
	150		2.8		2.5	
	200		2.9		2.6	
	300		2.9		2.7	
Device Operating Voltage (V_{DD})			+9		+5	V
Device Operating Current (I_{DD})			110	140	50.7	mA
DC Current Variation vs. Temperature[3]			-2.2		6.5	uA/°C
Device Current Variation Vs. Voltage			0.014[4]		0.013[5]	mA/mV

1. V_{DD} = +9 V tested on Mini-Circuits Package Characterization Test Board. V_{DD} = +5 V tested on Mini-Circuits Die Characterization Test Board. Board loss de-embedded.
2. Defined as Output Power at which gain is compressed by 1dB.
3. (Current at +85°C - Current at -45°C)/(+130°C)
4. (Current at +9.5 V - Current at +8.5 V) / (+9.5 V - +8.5 V)
5. (Current at +5.25 V - Current at +4.75 V) / (+5.25 V - +4.75 V)

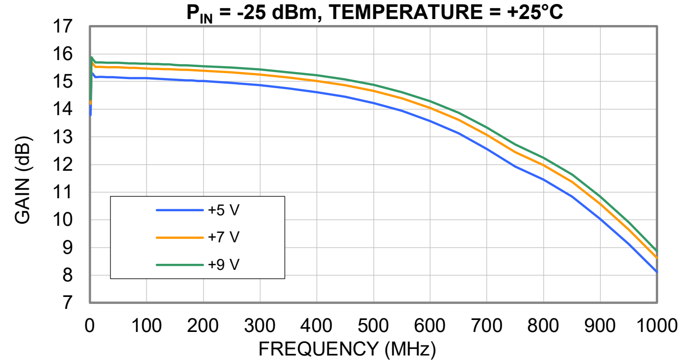
TYPICAL PERFORMANCE GRAPHS

Note: The following data was taken on package model PGA-32-75+ on the Mini-Circuits Characterization Test Board, TB-966+.
All data taken at nominal condition V_{DD} = +7 V unless noted otherwise.

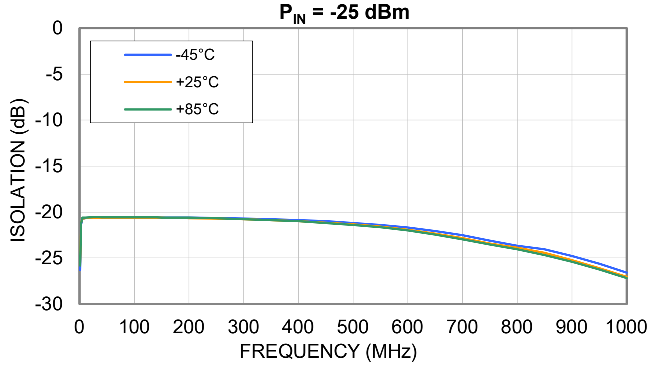
GAIN vs. TEMPERATURE
P_{IN} = -25 dBm



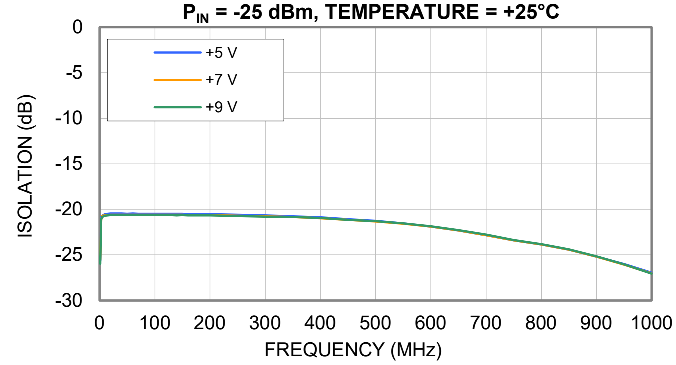
GAIN vs. DEVICE VOLTAGE (V_{DD})
P_{IN} = -25 dBm, TEMPERATURE = +25°C



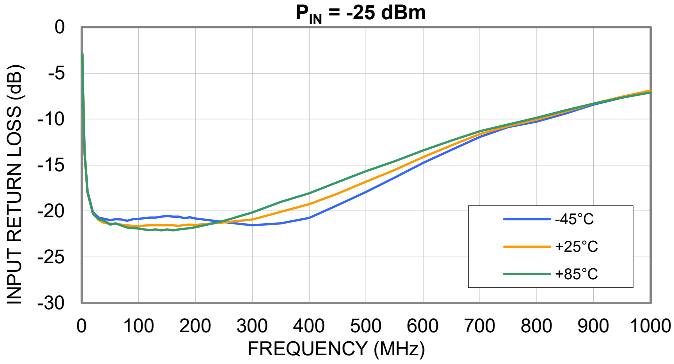
ISOLATION vs. TEMPERATURE
P_{IN} = -25 dBm



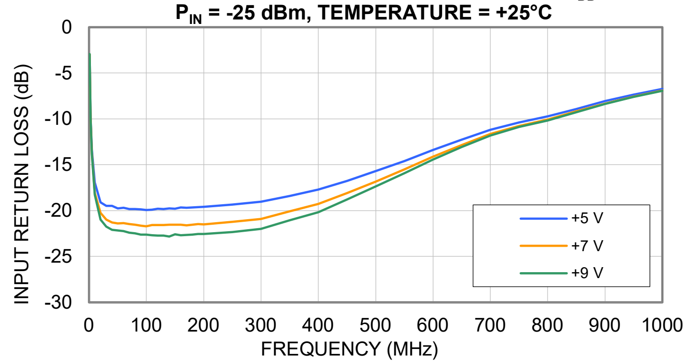
ISOLATION vs. DEVICE VOLTAGE (V_{DD})
P_{IN} = -25 dBm, TEMPERATURE = +25°C



INPUT RETURN LOSS vs. TEMPERATURE
P_{IN} = -25 dBm

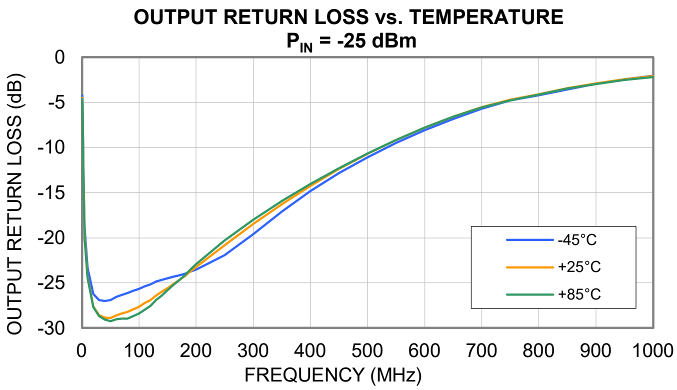


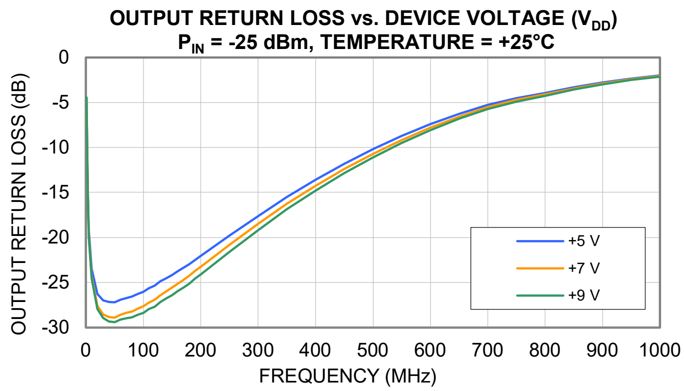
INPUT RETURN LOSS vs. DEVICE VOLTAGE (V_{DD})
P_{IN} = -25 dBm, TEMPERATURE = +25°C

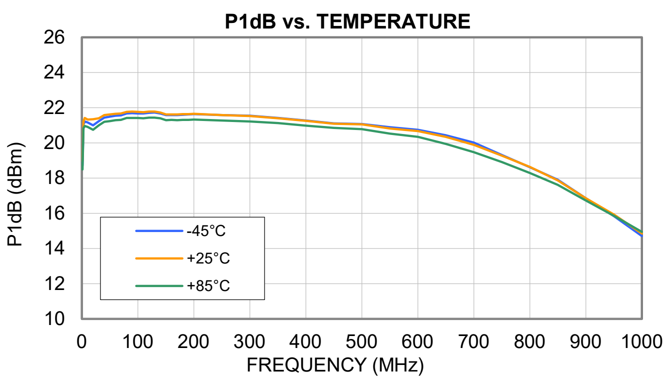


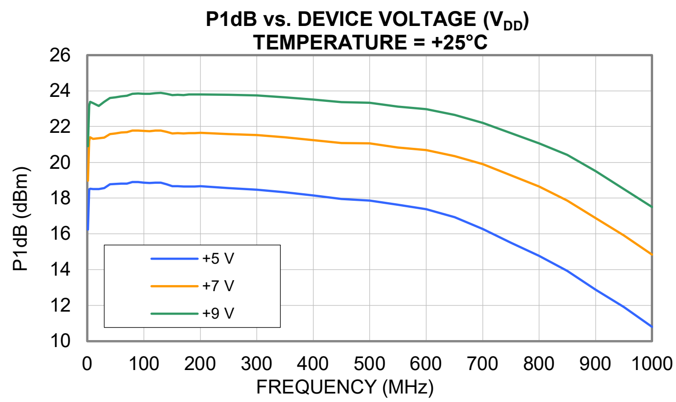
TYPICAL PERFORMANCE GRAPHS

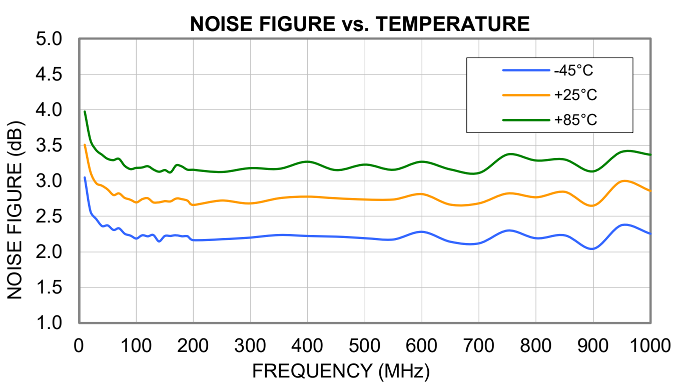
Note: The following data was taken on package model PGA-32-75+ on the Mini-Circuits Characterization Test Board, TB-966+.
All data taken at nominal condition V_{DD} = +7 V unless noted otherwise.

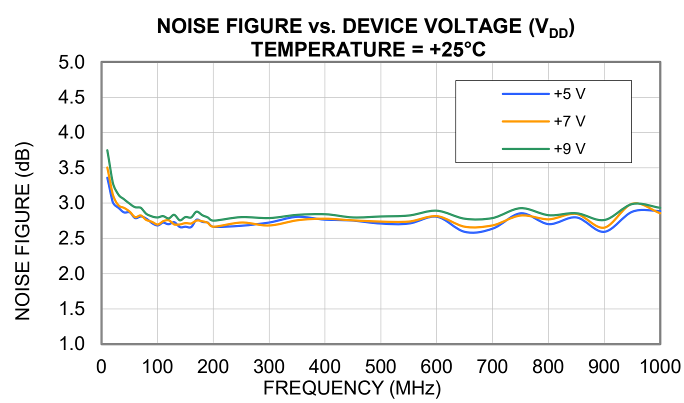






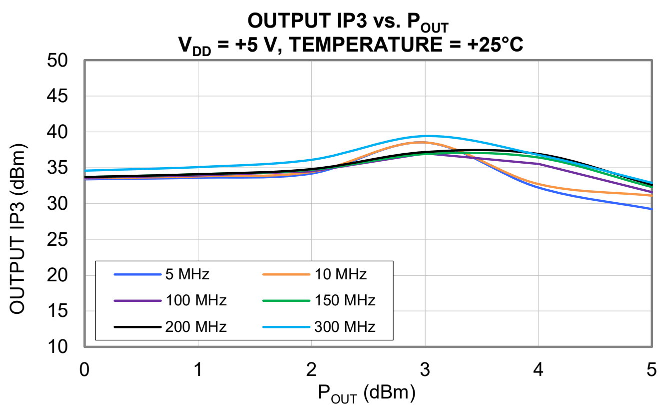


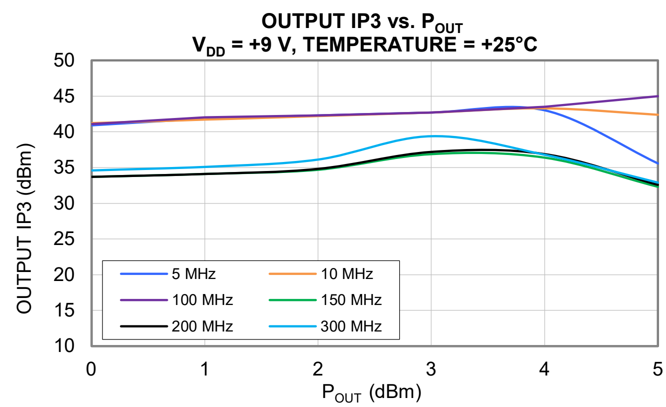




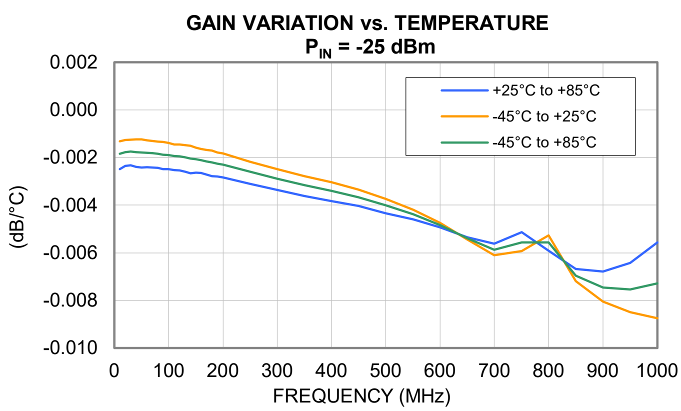
TYPICAL PERFORMANCE GRAPHS

Note: The following data was taken on die model PGA-32-75-D+ on the Mini-Circuits Characterization Test Board, TB-966+.





Note: The following data was taken on package model PGA-32-75+ on the Mini-Circuits Characterization Test Board, TB-966+.
All data taken at nominal condition V_{DD} = +7 V unless noted otherwise.



ABSOLUTE MAXIMUM RATINGS[6]

Parameter	Ratings
Operating Temperature[7]	-45°C to +85°C
Storage Temperature (for Die)[8]	-65°C to +150°C
Junction Temperature[9]	+150°C
Total Power Dissipation	2.2 W
Input Power (CW), V_{DD} = +9 V	+23 dBm
DC Voltage on Pad 2 (V_{DD})	+11 V

6. Permanent damage may occur if these limits are exceeded. Maximum ratings are not intended for continuous normal operation.
7. Bottom of Die.
8. For die shipped in Gel-Pak see ENV80 (limited by packaging).
9. Peak temperature on top of Die.

THERMAL RESISTANCE

Parameter	Ratings
Thermal Resistance (Θ_{JC})[10]	30°C/W

10. Θ_{JC}= (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

ESD RATING[11]

	Class	Voltage Range	Reference Standard
HBM	1A	250 V to <500 V	ANSI/ESDA/JEDEC JS-001-2017
MM	M1	+25 V	ANSI/ESD STM5.2-1999

ESD HANDLING PRECAUTION: This device is designed to be Class 1A for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage.

11. Data taken on packaged model PGA-32-75+.

FUNCTIONAL DIAGRAM

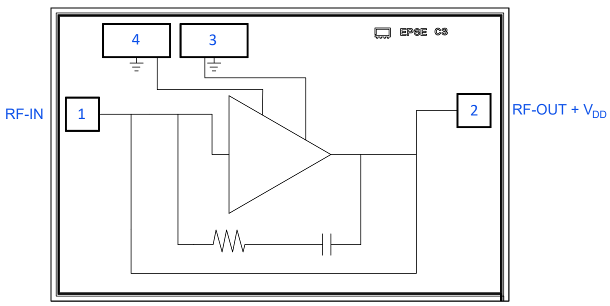


Figure 1. PGA-32-75-D+ Functional Diagram

PAD DESCRIPTION

Function	Pad Number	Application Description (Refer to Figure 3)
RF-IN	1	RF-IN pad connects to RF Input port.
RF-OUT + V_{DD}	2	RF-OUT pad connects to RF Output port and voltage input port, V_{DD}.
GND	3,4	Bond wires to ground are required. See Assembly Diagram figure 4 below.

DIE OUTLINE: inches [mm], Typical

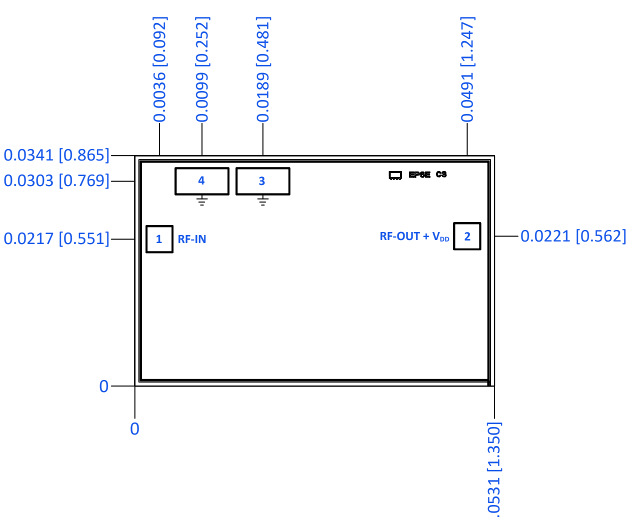


Figure 2. PGA-32-75-D+ Die Outline

DIMENSIONS: inches [mm], Typical

Die Size	0.0531 x 0.0341 [1.350 x 0.865]
Die Thickness	0.0040 [0.100]
Bond Pad Sizes:	
Pads 1, 2	0.0037 x 0.0037 [0.094 x 0.094]
Pads 3, 4	0.0076 x 0.0037 [0.194 x 0.094]
Plating (Pads & Bottom of Die)	Gold

CHARACTERIZATION BOARD

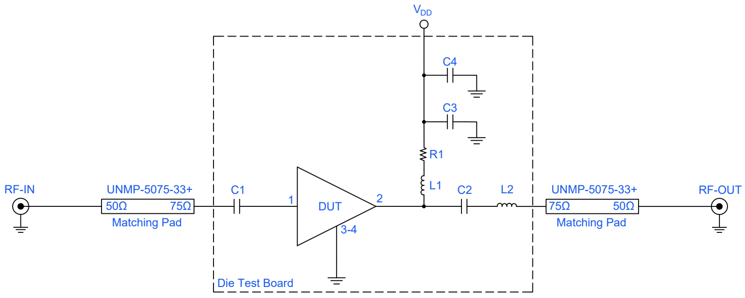


Figure 3. PGA-32-75-D+ Characterization Circuit

Electrical Parameters and Conditions
Gain, Return Loss, Output Power at 1dB Compression (P1dB), Output IP3 (OIP3), Output IP2 (OIP2), and Noise Figure measured using N5242A PNA-X Microwave Network and E5071C ENA Series Network Analyzer.

Conditions:
1. Gain and Return Loss: P_{IN} = -25 dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, +5 dBm/tone at output.
3. Output IP2 (OIP2): Two tones, spaced 1 MHz apart, +5 dBm/tone at output.

Component	Value	Size	Part Number	Manufacturer
C1, C4	0.1 µF	0402	GRM155R71C104KA88D	Murata
C2	0.01 µF	0402	GRM155R71E103KA01D	Murata
C3	0.001 µF	0402	GRM1555C1H102JA01D	Murata
L1	6800 nH	1210	LQH32MN6R8K23L	Murata
L2	12 nH	0402	LQW15AN12NH00D	Murata
R1	4.99Ω	0603	RK73H1JTTD4R99F	KOA Speer

ASSEMBLY DIAGRAM

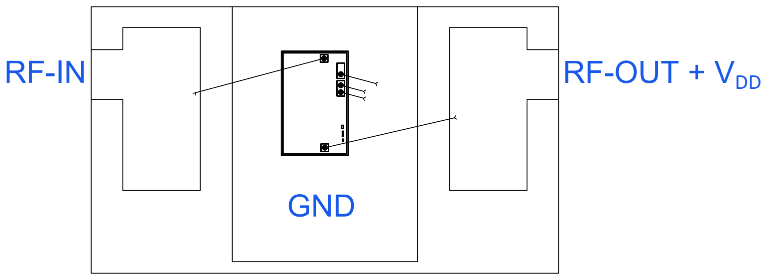


Figure 4. PGA-32-75-D+ Assembly Diagram

Refer to the table in Figure 3 for more details on the passive components.

- Bond wire diameter: 1 mil
- Bond wire lengths from Die pad to PCB at RF-IN and RF-OUT + V_{DD} pads: 67 ± 2 mils
- Bond wire lengths from Die pad to PCB at GND pads: 18 ± 2 mils
- Typical Gap from Die Edge to PCB edge: 3 mils
- PCB thickness and material: 20 mils FR4 (Thickness: 1 oz copper on each side)

ASSEMBLY AND HANDLING PROCEDURE

1. Storage
   Die should be stored in a dry nitrogen purged desiccator or equivalent.
2. ESD Precautions
   MMIC E-pHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in anti-static protected material, which should be opened only in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
   Devices require careful handling using tools appropriate for manipulating semiconductor chips. It is recommended to handle the chips along the edges with a custom designed collet. The die mounting surface must be clean and flat. Using conductive silver-filled epoxy, apply sufficient adhesive to meet the required bond line thickness, fillet height and coverage around the total periphery of the device. The recommended epoxy is Ablestik 84-1 LMISR4 or equivalent. Parts should be cured in a nitrogen-filled atmosphere per manufacturer's recommended cure profile.
4. Wire Bonding
   Openings in the surface passivation above the gold bond pads are provided to allow wire bonding to the die. Thermosonic bonding is recommended with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. The suggested interconnect is pure gold, 1 mil diameter wire. Bonds are recommended to be made from the bond pads on the die to the package or substrate. All bond wire length and bond wire height should be kept as short as possible, unless specified by design, to minimize performance degradation due to undesirable series inductance.

ADDITIONAL DETAILED INFORMATION IS AVAILABLE ON OUR DASHBOARD

CLICK HERE

Performance Data & Graphs	Data Graphs S-Parameter (S2P Files) Data Set (.zip file)	
Case Style	Die	
RoHS Status	Compliant	
Die Ordering and Packaging Information	Quantity, Package	Model No.
	Gel - Pak: 5, 10, 100 KGD*	PGA-32-75-DG+
	Medium†, Partial wafer: KGD*<1344	PGA-32-75-DP+
	Full wafer†	PGA-32-75-DF+
	†Available upon request contact sales representative. Refer to AN-60-067	
Die Marking	EP6E_C3	
Environmental Ratings	ENV80	

* Known Good Die ("KGD") means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within a predefined range. While DC testing is not definitive, it does provide a high degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.