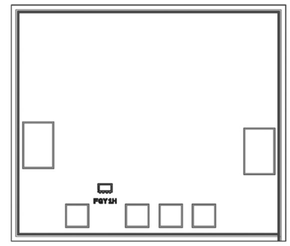
Ultra High Dynamic Range

Monolithic Amplifier Die **PHA-83W-D+**

50Ω 50 MHz to 8 GHz



The Big Deal

- Ultra Wideband, 0.05 - 8 GHz
- Excellent Gain Flatness 15.7±1.4 dB Typ.
- High Linearity, +23.3 dBm P1dB & +35.5 dBm OIP3
- Robust ESD performance (Class 1B)

Product Overview

PHA-83W-D+ (RoHS compliant) is an advanced wideband amplifier die fabricated using PHEMT technology and offers extremely high dynamic range over a broad frequency range and with excellent gain flatness. In addition, the PHA-83W-D+ has good input and output return loss over a broad frequency range.

Key Features

Feature	Advantages
Ultra Wideband: 50 MHz to 8 GHz	Broadband covering primary wireless communications bands
Extremely High IP3: 36.6 dBm typ. at 50 MHz 37 dBm typ. at 6 GHz	The PHA-83W-D+ matches industry leading IP3 performance relative to device size and power consumption. The combination of the design and PHEMT Structure provides enhanced linearity over a broad frequency range as evidence in the IP3 being approximately 12 dB above the P1dB point. This feature makes this amplifier ideal for use in: •Driver amplifiers for complex waveform up converter paths •Drivers in linearized transmit systems •Secondary amplifiers in ultra-High Dynamic range receivers
Excellent Gain Flatness	Typical ±1.4dB gain flatness across the entire frequency range minimizes the need for external equalizer networks making it a great fit for instrumentation and EW application.
Unpackaged Die	Enables the user to integrate the amplifier directly into hybrids

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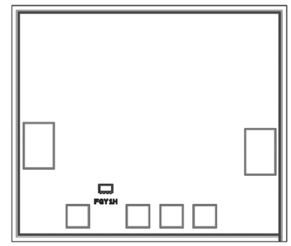

Product Features

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- Excellent Gain Flatness 15.7±1.4dB Typ.
- High Linearity, +23.3 dBm P1dB & +35.5 dBm OIP3
- Robust ESD performance (Class 1B)

Typical Applications

- WiFi
- WLAN
- LTE
- WiMAX
- S-band Radar
- C-Band Satcom

+RoHS Compliant

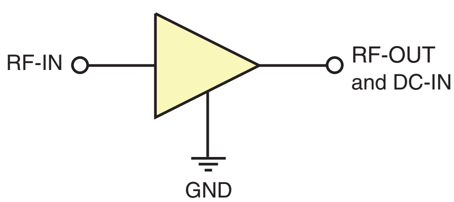
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Ordering Information: Refer to Last Page

General Description

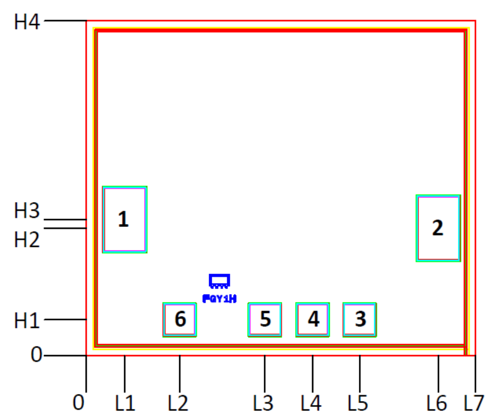
PHA-83W-D+ (RoHS compliant) is an advanced wideband amplifier fabricated using PHEMT technology and offers extremely high dynamic range over a broad frequency range and with excellent gain flatness. In addition, the PHA-83W-D+ has good input and output return loss over a broad frequency range.

Simplified Schematic and Pad description



Pad#	Description
1	RF-IN
2	RF-OUT & DC-IN
3,4,5,6	GND

Bonding Pad Position



Dimensions in µm, Typical

L1	L2	L3	L4	L5	L6	L7	H1	H2	H3	H4
88	214	410	518	626	807	892	82	209	312	767

Thickness	Die size	Pad Size 1 & 2	Pad size 3,4,5&6
100	892 x 767	94 x 144	69 x 69

Electrical Specifications at 25°C, 50Ω, unless noted

Parameter	Condition (MHz)	V_{DD}=9V[1]			V_{DD}=5V[1]	V_{DD}=9V[2]	V_{DD}=5V[2]	Units
		Min.	Typ.	Max.	Typ.	Typ.	Typ.	
Frequency range		50		8000	50-8000	50-8000	50-8000	MHz
Gain	50		16.7		15.1	16.3	14.9	dB
	2000		16.3		14.4	16	14.2	
	4000		15.7		13.2	15.3	12.8	
	6000		16		12.6	15.5	12.4	
	8000		14.2		10	12.4	8.2	
Gain flatness	50 - 8000		1.4		2.8	—	—	dB
Input return loss	50		23		20	16	16	dB
	2000		21		14	21	17	
	4000		13		11	14	12	
	6000		13		14	14	16	
	8000		4		6	3	5	
Output return loss	50		17		26	13	17	dB
	2000		30		17	33	22	
	4000		18		13	17	12	
	6000		18		12	15	20	
	8000		5		6	6	6	
Output power @1 dB compression	50		23.8		16.5	23.7	15.6	dBm
	2000		23.8		16.3	24.3	16	
	4000		23.3		15.9	22.6	14.1	
	6000		22.6		16.4	22.6	15.8	
	8000		18.5		13.2	16.7	11	
Output IP3 (Pout= 0dBm/Tone)	50		36.6		24.1	36.5	25.9	dBm
	2000		36		23.4	35.4	24.6	
	4000		35.5		23.4	34.5	22.8	
	6000		37		23.6	35.6	25.1	
	8000		31.9		20.9	29.9	19.5	
Noise figure	50		3.3		2.8	3.4	2.8	dB
	2000		2.9		2.7	2.9	2.7	
	4000		3.3		3.1	3.5	3.1	
	6000		3.9		3.6	3.9	3.5	
	8000		5.1		4.7	5.4	4.9	
Device operating voltage		8.5	9	9.5	5	9	5	V
Device operating current			110	127	40.8	115	42.7	mA
Device current variation vs. temperature[3]			34.6		30.8	34.6	30.8	μA/°C
Device current variation vs voltage[4]			0.018		0.015	0.018	0.015	mA/mV
Thermal resistance, junction-to-ground Lead at 85°C stage temperature			41		41	41	41	°C/W

1. Die is packaged in SOT-89 and soldered on TB-PHA-83W+. See Characterization Test Circuit (Figure 1).
2. Die is packaged in SOT-89 and soldered on TB-PHA-83WE+. See Application Test Circuit (Figure 2).
3. Device Current Variation vs. Temperature= (Current at 85°C - Current at -45°C)/130
4. Device Current Variation vs. Voltage = (Current at 9.5V - Current at 8.5V) / ((9.5V-8.5V)*1000 mV/V)

Absolute Maximum Ratings[5]

Parameter	Ratings
Operating temperature (ground lead)	-40°C to 85°C
Power dissipation	1.58W
Input power (CW)	18 dBm (continuous) 24 dBm (5 minutes max)
DC Voltage or V_{DD}	10.5V

Characterization Test Circuit

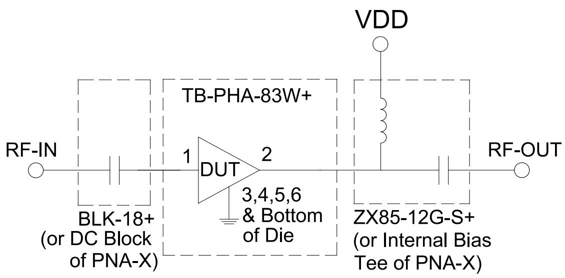
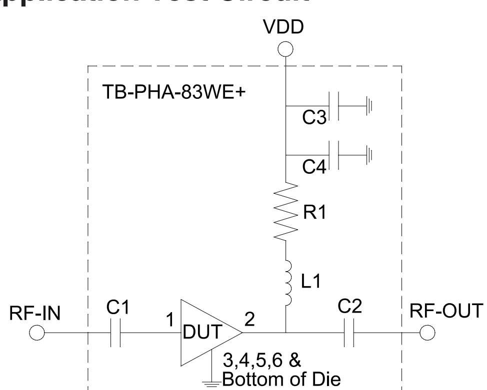


Fig 1. Block Diagram of Test Circuit used for characterization. (DUT is packaged in SOT-89 and soldered on Mini-Circuits Characterization test board TB-PHA-83W+) Gain, Return loss, Output power at 1dB compression (P1 dB) , output IP3 (OIP3) and noise figure measured using Agilent's N5242A PNA-X microwave network analyzer.

Conditions:
1. Gain and Return loss: Pin= -25dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 0 dBm/tone at output.

Application Test Circuit

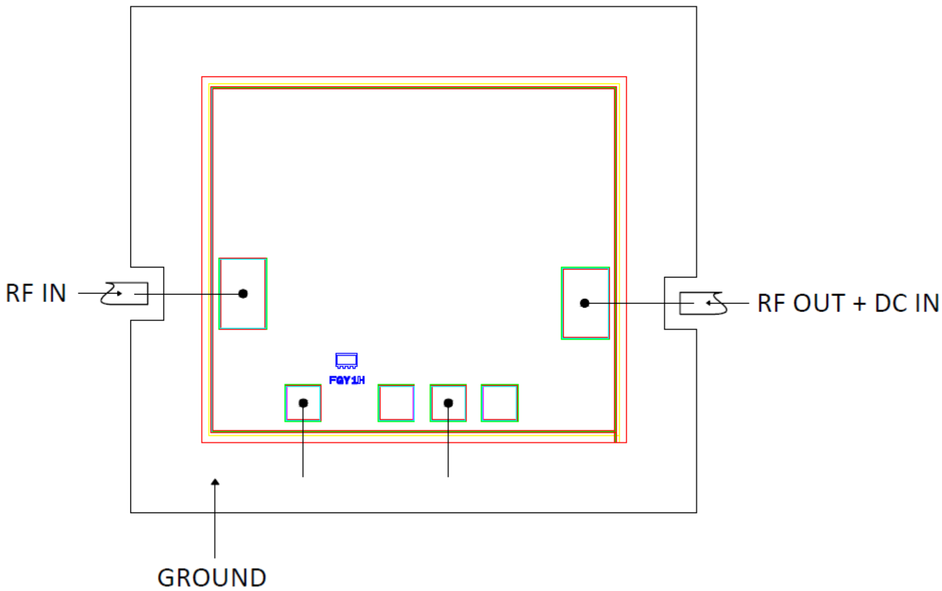


Component	Size	Value	Part Number	Manufacturer
C1	0402	1000pF	GRM1555C1H102JA01D	Murata
C2	0402	180pF	GRM1555C1H181JA01D	Murata
C3	0402	0.1 uF	GRM155R71C104KA88D	Murata
C4	0402	10000pF	GRM155R71E103KA01D	Murata
L1	0603	330nH	LQW18CNR33J00D	Murata
R1	0402	20hm	RK73H1ETTP2R00F	Koa

Fig 2. Block Diagram of Test Circuit used for characterization. (DUT is packaged in SOT-89 & soldered on Mini-Circuits Application test board TB-PHA-83WE+)
Gain, Return loss, Output power at1dB compression (P1dB), output IP3 (OIP3) and noise figure measured using Agilent's N5242A PNA-X microwave network analyzer.

Conditions:
1. Gain and Return loss: Pin= -25dBm
2. Output IP3 (OIP3): Two Tones spaced 1 MHz apart, 0 dBm/ tone at output.

Assembly Diagram



Assembly and Handling Procedure

1. Storage
   Dice should be stored in a dry nitrogen purged desiccators or equivalent.
2. ESD
   MMIC PHEMT amplifier dice are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic protected material, which should be opened in clean room conditions at an appropriately grounded anti-static worksta tion. Devices need careful handling using correctly designed collets, vacuum pickup tips or sharp antistatic tweezers to deter ESD damage to dice.
3. Die Attach
   The die mounting surface must be clean and flat. Using conductive silver filled epoxy, recommended epoxies are DieMat DM6030HK-PT/H579 or Ablestik 84-1LMISR4. Apply sufficient epoxy to meet required epoxy bond line thickness, epoxy fillet height and epoxy coverage around total die periphery. Parts shall be cured in a nitrogen filled atmosphere per manufacturer's cure condition. It is recommended to use antistatic die pick up tools only.
4. Wire Bonding
   Bond pad openings in the surface passivation above the bond pads are provided to allow wire bonding to the dice gold bond pads. Thermosonic bonding is used with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. Suggested wire is pure gold, 1 mil diameter. Bonds must be made from the bond pads on the die to the package or substrate. All bond wires should be kept as short as low as reasonable to minimize performance degradation due to undesirable series inductance.

Additional Detailed Technical Information *additional information is available on our dash board.*	
Performance Data	Data Table
	Swept Graphs
	S-Parameter (S2P Files) Data Set with and without port extension(.zip file)
Case Style	Die
Die Ordering and packaging information	Quantity, Package — Model No. Small, Gel - Pak: 5,10,50,100 KGD* — PHA-83W-DG+ Medium†, Partial wafer: KGD*<1845 — PHA-83W-DP+ Large†, Full Wafer — PHA-83W-DF+ †*Available upon request contact sales representative* Refer to AN-60-067
Environmental Ratings	ENV80

*Known Good Dice ("KGD") means that the dice in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such dice fall within a predefined range. While DC testing is not definitive, it does help to provide a higher degree of confidence that dice are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

ESD Rating**

Human Body Model (HBM): Class 1B (pass 500V) in accordance with ANSI/ESD STM 5.1 - 2001

** Tested in industry standard SOT-89 package.

Additional Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.

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