



MMIC SURFACE MOUNT

Power Amplifier

PHA2-13HLN+

50Ω 10 to 500 MHz Dual Matched Amplifier

THE BIG DEAL

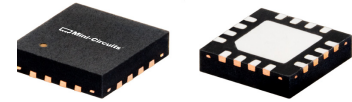
- Dual Matched Amplifier
- Gain, Typ. 21.8 dB
- OIP2, Typ. +88 dBm
- Noise Figure, Typ. 1.8 dB
- Output P1dB, Typ. +30.2 dBm
- DC Supply +8 V at 490 mA
- 4x4 mm 16-Lead QFN-Style Package

APPLICATIONS

- Broadcasting
- Aeronautical Radionavigation
- VHF
- Satellite Communications

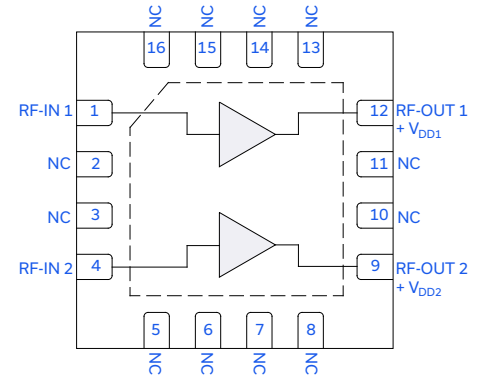
PRODUCT OVERVIEW

Mini-Circuits' PHA2-13HLN+ is a dual-matched E-pHEMT-based wideband MMIC power amplifier with high gain and high output IP2 when implemented in a balanced configuration. Operating from 10 to 500 MHz, this amplifier features typical 1.8 dB noise figure, 21.8 dB gain, +30.2 dBm P1dB, and +88 dBm OIP2. This device requires a +8 V supply voltage for each amplifier path and is matched to 50Ω in a small 4x4 mm 16-Lead QFN-style package for easy integration into dense circuit board layouts.



Generic photo used for illustration purposes only

FUNCTIONAL DIAGRAM (TOP VIEW)



KEY FEATURES

Feature	Advantages
Noise Figure, Typ. 1.8 dB	A 50Ω matched low noise MMIC device enables low system noise figure performance without the need for complicated discrete-based solutions.
High P1dB Typ. +30.2 dBm	Flat gain and output power make this device excellent for wideband systems from 10 to 500 MHz that require at least 1 W of operating output power over the full band.
High OIP3 Typ. +49 dBm High OIP2 Typ. +88 dBm	High operating OIP3, OIP2, as well as low 2nd and 3rd harmonic responses, provides very low in-band distortion products optimized for high fidelity measurement systems.
4x4 mm 16-Lead QFN-Style Package	Small footprint saves space in dense PCB layouts while providing low inductance, repeatable transitions, and excellent thermal contact with the PCB. Industry standard packaging allows for easy assembly in high volume manufacturing processes.

REV. OR
ECO-027127
PHA2-13HLN+
MCL NY
250925





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ELECTRICAL SPECIFICATIONS AT +25°C, $V_{DD1} = V_{DD2} = +8\text{ V}$, $Z_0 = 50\Omega$ UNLESS NOTED OTHERWISE

Parameter	Condition (MHz)	PHA2-13HLN+ (Application specific) ¹			Units
		Min.	Typ.	Max.	
Frequency Range		10		500	MHz
Gain	10	23.3	24.3		dB
	30	22.3	23.3		
	50	22.0	22.9		
	200	21.0	21.8		
	500	18.1	19.0		
Input Return Loss	10		16		dB
	30		17		
	50		17		
	200		11		
	500		6		
Output Return Loss	10		29		dB
	30		19		
	50		17		
	200		10		
	500		6		
Isolation	10-500		27		dB
Output Power at 1 dB Compression (P1dB)	10		+28.7		dBm
	30		+30.1		
	50		+30.3		
	200		+30.2		
	500		+27.2		
Output Second-Order Intercept ($P_{OUT} = +10\text{ dBm/Tone}$)	10		+93		dBm
	30		+99		
	50		+99		
	200		+88		
	500		+72		
Output Third-Order Intercept ($P_{OUT} = +10\text{ dBm/Tone}$)	10		+46		dBm
	50		+47		
	500		+49		
Noise Figure	10		2.3		dB
	30		1.6		
	50		1.6		
	200		1.8		
	500		2.9		
Device Operating Voltage (V_{DD}) ²		+7.75	+8.0	+8.25	V
Device Operating Current (I_{DD}) ³			497		mA
DC Current Variation vs. Temperature ⁴			-137.5		$\mu\text{A}/^\circ\text{C}$
DC Current Variation vs. Voltage ⁵			0.064		mA/mV

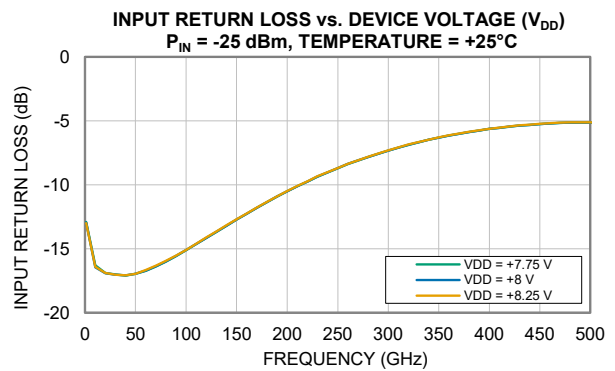
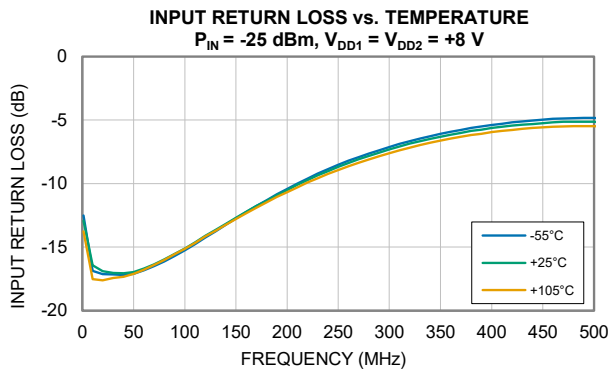
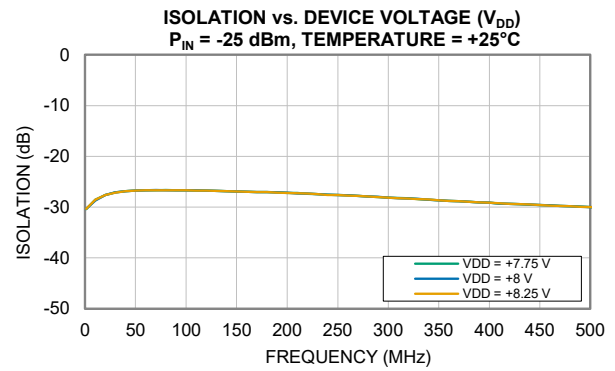
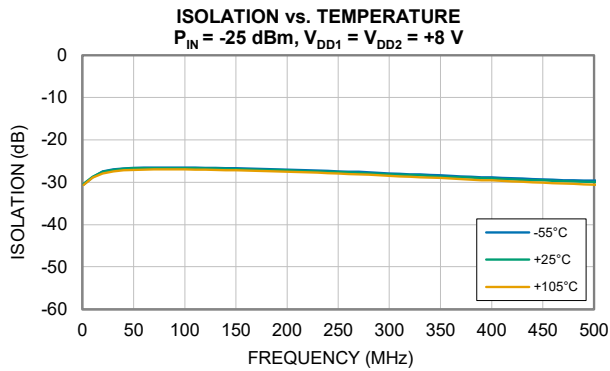
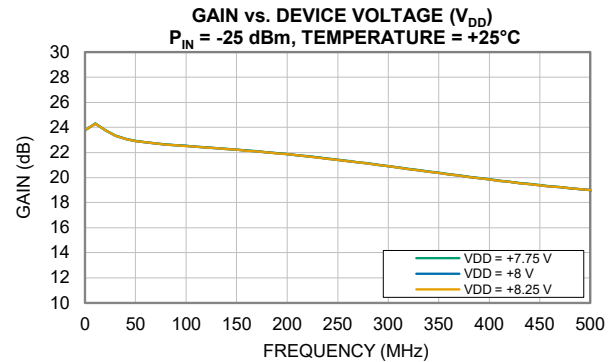
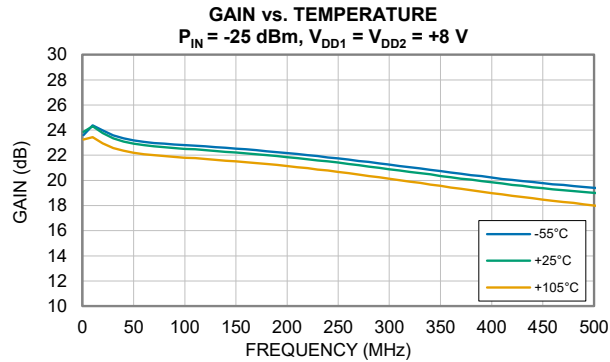
1. Tested on Mini-Circuits Characterization Test Board TB-PHA2-13HLNC+. See Figure 2.

2. $V_{DD} = V_{DD1} = V_{DD2}$ 3. Current at $P_{IN} = -25\text{ dBm}$. Current I_{DD} decreases to 490 mA at P1dB when $V_{DD} = +8\text{ V}$ 4. $(\text{Current at } +105^\circ\text{C} - \text{Current at } -55^\circ\text{C}) / (+105^\circ\text{C} - -55^\circ\text{C})$ 5. $(\text{Current at } +8.25\text{ V} - \text{Current at } +7.75\text{ V}) / (+8.25\text{ V} - +7.75\text{ V})$ 



TYPICAL PERFORMANCE GRAPHS

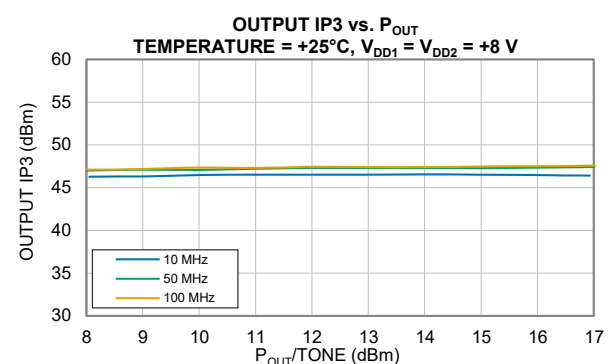
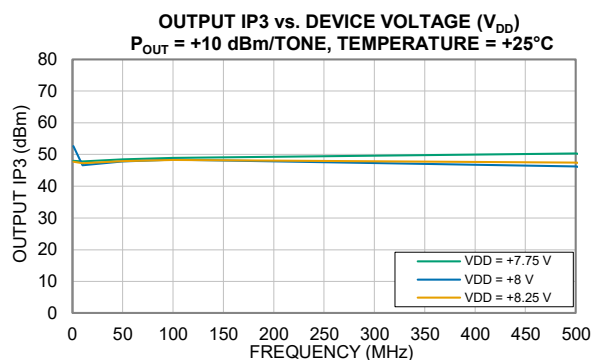
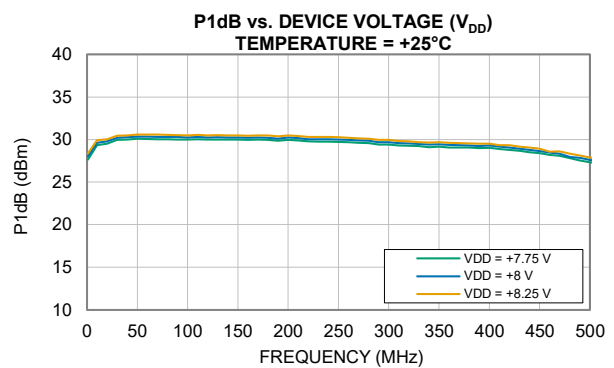
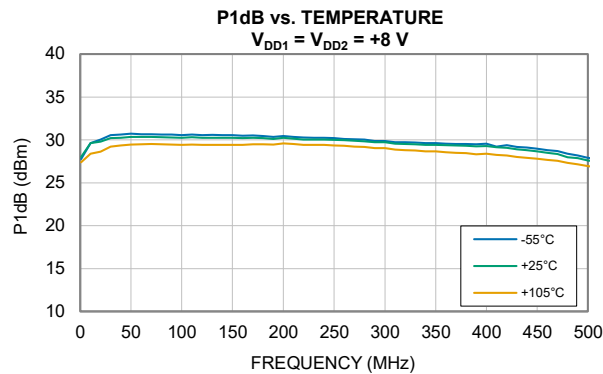
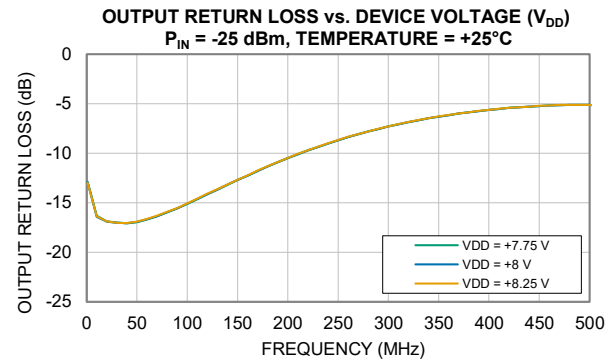
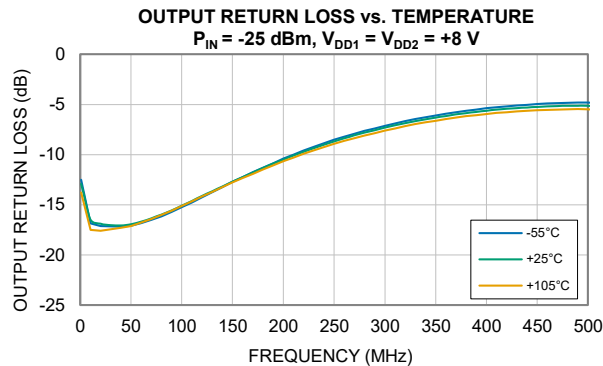
Note: The following data was taken on the Mini-Circuits Characterization Test Board TB-PHA2-13HLNC+ (Figure 2).
All data taken at nominal conditions $V_{DD1} = V_{DD2} = +8\text{ V}$ unless noted otherwise.





TYPICAL PERFORMANCE GRAPHS

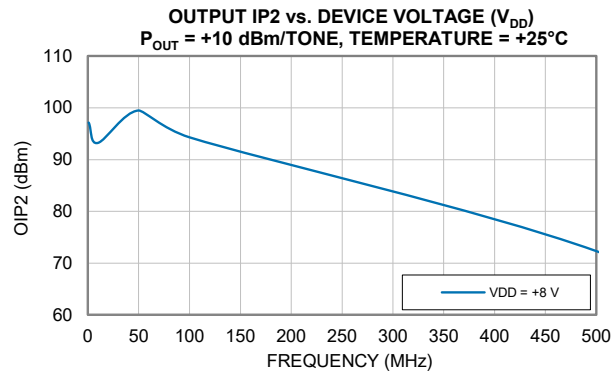
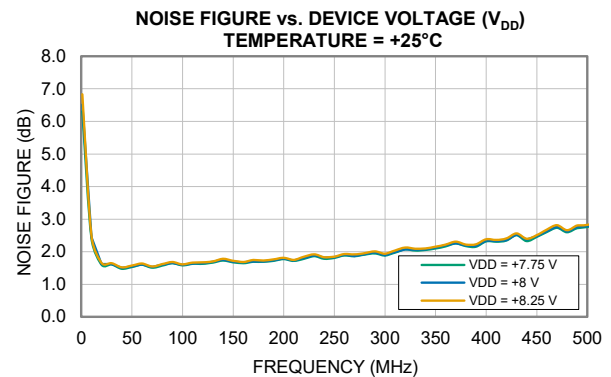
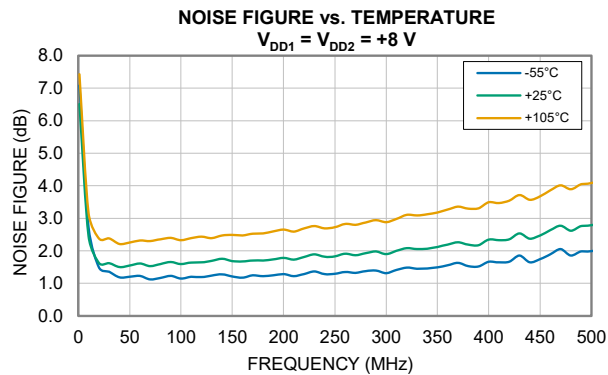
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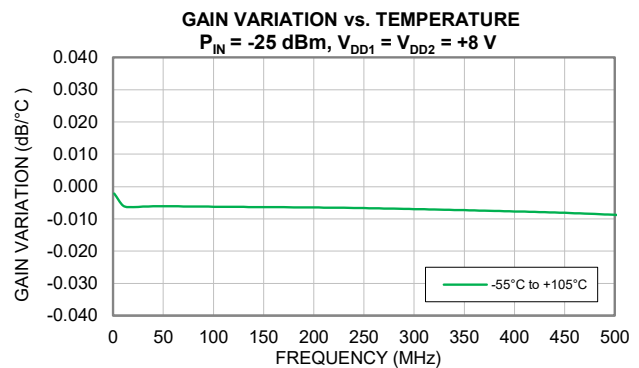
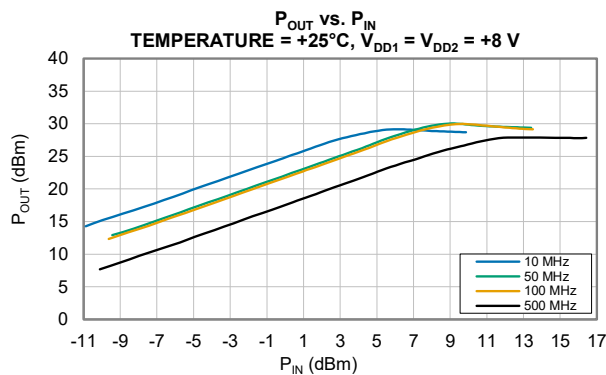
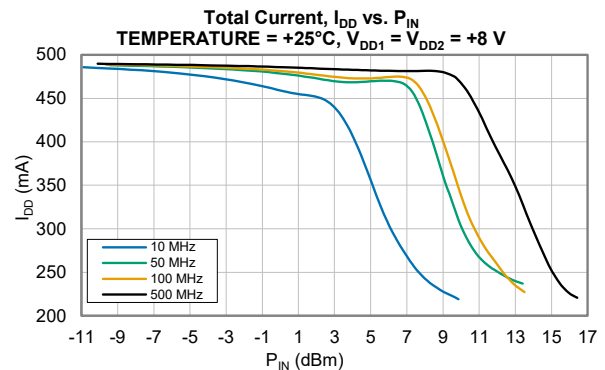
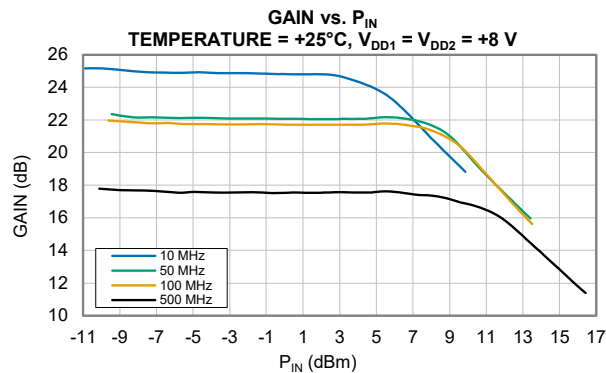
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TYPICAL PERFORMANCE GRAPHS

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ABSOLUTE MAXIMUM RATINGS⁶

Parameter	Ratings
Operating Temperature	-55°C to +105°C
Storage Temperature	-65°C to +150°C
Junction Temperature ⁷	+150°C
Total Power Dissipation	2.25 W
Input Power (CW), $V_{DD} = +8$ V	+25 dBm
DC Drain Voltage on V_{DD1}	+20 V
DC Drain Current on I_{DD1}	338 mA
DC Drain Voltage on V_{DD2}	+20 V
DC Drain Current on I_{DD2}	328 mA

6. Permanent damage may occur if any of these limits are exceeded. Maximum ratings are not intended for continuous normal operation.

7. Peak temperature on top of Die.

ABSOLUTE MAXIMUM RATINGS⁸

Parameter	Ratings
DC Voltage on RF-OUT, $V_{DD} = +8$ V	+0.5 V
DC Current on RF-OUT, $V_{DD} = +8$ V	1000 mA
DC Voltage on RF-IN, $V_{DD} = +8$ V	+0.5 V
DC Current on RF-IN, $V_{DD} = +8$ V	1000 mA

8. Tested on Mini-Circuits characterization test board TB-PHA2-13HLNC+. See figure 2

THERMAL RESISTANCE

Parameter	Ratings
Thermal Resistance (θ_{JC}) ⁹	19.8°C/W

9. θ_{JC} = (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

ESD RATING

	Class	Voltage Range	Reference Standard
HBM	1B	500 V to < 1000 V	ANSI/ESD STM 5.1 - 2001
CDM	C3	> 1000 V	ANSI/ESDA/JEDEC JS-002-2022



ESD HANDLING PRECAUTION: This device is designed to be Class 1B for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage.

MSL RATING

Moisture Sensitivity: MSL1 in accordance with IPC/JEDEC J-STD-020D /JEDEC J-STD-033C





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FUNCTIONAL DIAGRAM (TOP VIEW)

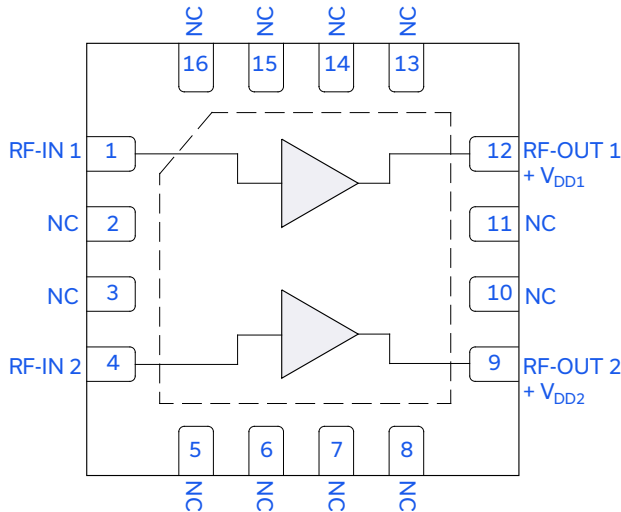


Figure 1. PHA2-13HLN+ Functional Diagram

PAD DESCRIPTION

Function	Pad Number	Description (Refer to Figure 2)
RF-IN 1	1	RF-IN 1 pad connects to RF-Input port 1.
RF-IN 2	4	RF-IN 2 pad connects to RF-Input port 2.
RF-OUT 1 + V _{DD1}	12	RF-OUT 1 Pad connects to RF Output port 1. V _{DD1} is applied via external bias tee.
RF-OUT 2 + V _{DD2}	9	RF-OUT 2 Pad connects to RF Output port 2. V _{DD2} is applied via external bias tee.
GND	Paddle	Connects to ground.
NC	2, 3, 5-8, 10, 11, 13-16	Not used internally. Connected to ground on test board.

CHARACTERIZATION TEST BOARD

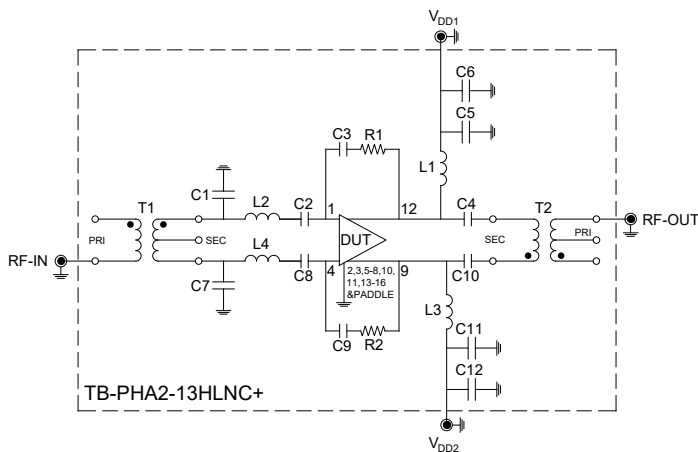


Figure 2. PHA2-13HLN+ Characterization and Application Circuit

Electrical Parameters and Conditions

Gain, Return Loss, Output Power at 1dB Compression (P1dB), Output IP3 (OIP3), and Noise Figure measured using N5247B PNA-X Microwave Network Analyzer.

Conditions:

- Gain and Return Loss: $P_{IN} = -25$ dBm
- Output IP3 (OIP3): Two tones, spaced 1 MHz apart, +10 dBm/Tone at output.

Power ON/Power OFF Sequence:

PHA2-13HLN+ is not sensitive to power ON/OFF sequence. V_{DD1} and V_{DD2} can be applied in any order. The V_{DD1} and V_{DD2} voltage lines may be tied together and applied simultaneously

Component	Value	Size	Part Number	Manufacturer
C1, C7	1.5 pF	0402	GRM1555C1H1R5CA01D	MURATA
C2, C4, C8, C10	2.2 μ F	0603	GRM188C71E225KE11D	MURATA
C3, C9	0.1 μ F	0402	GRM155R71C104KA88D	MURATA
C5, C11	1000 pF	0402	GRM1555C1H102JA01D	MURATA
C6, C12	10 μ F	0805	GRM21BC71E106KE11L	MURATA
L1, L3	15 μ H	1210	LQH32DN150K53L	MURATA
L2, L4	5.1 nH	0603	0603CS-5N1XJLW	COILCRAFT
R1, R2	1.5 KOhm	0402	RK73H1ETTP1501F	KOA SPEER
T1, T2	1:2	7.87 x 5.58 mm	ADT2-1T+	MINI-CIRCUITS

Mini-Circuits



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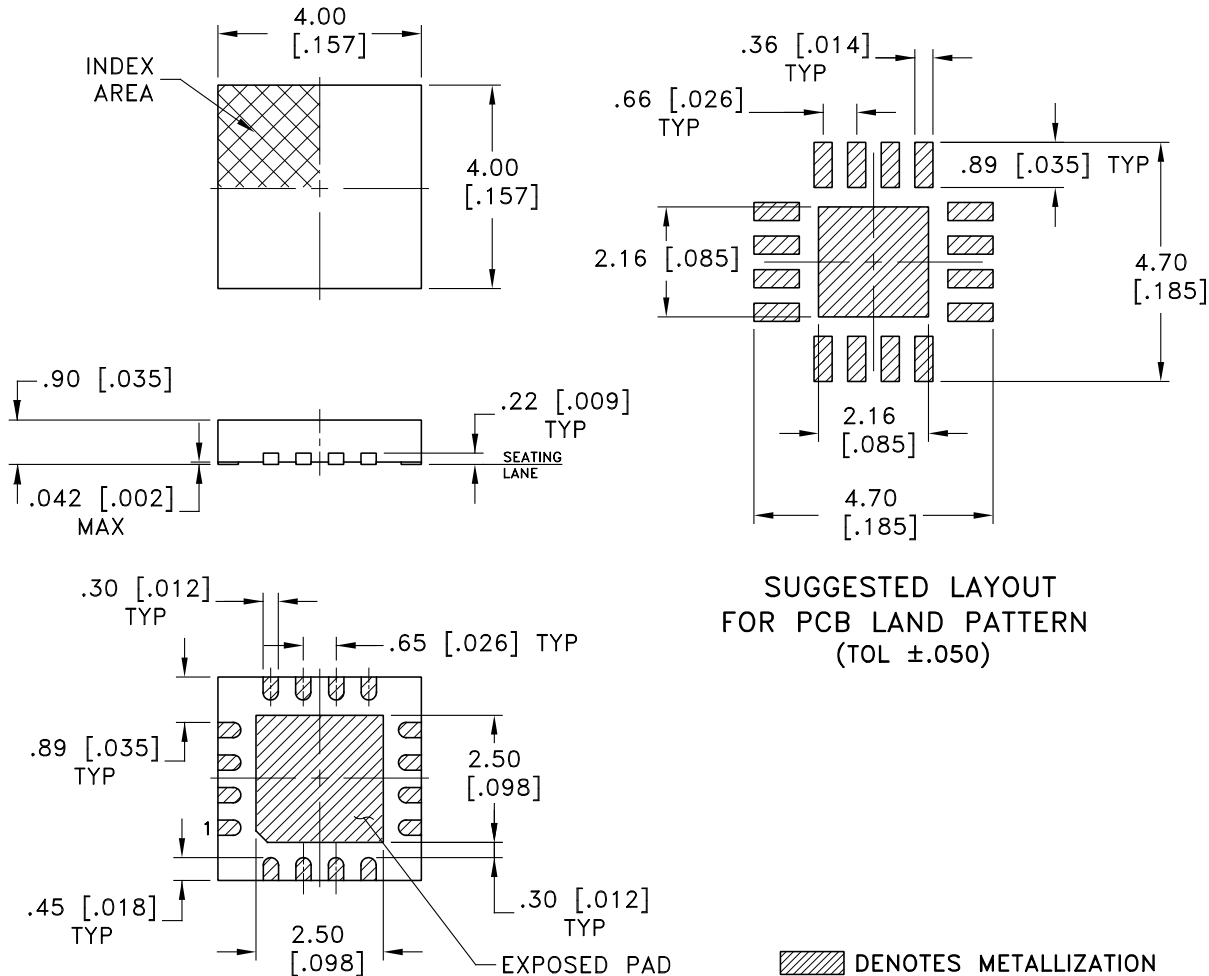
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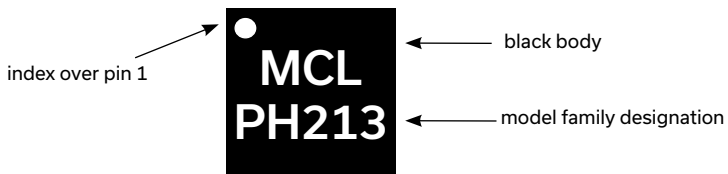
CASE STYLE DRAWING



Weight: 0.04 grams

Dimensions are in mm [inches]. Tolerances: 2 Pl. ± 0.0127 mm; 3 Pl. ± 0.025 mm

PRODUCT MARKING



Marking may contain other features or characters for internal lot control

Mini-Circuits



Mini-Circuits®

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ADDITIONAL DETAILED TECHNICAL INFORMATION IS AVAILABLE ON OUR DASHBOARD. [CLICK HERE](#)

Performance Data	Data Table Swept Graphs S-Parameter (S2P Files) Data Set (.zip file)
RoHS Status	Compliant
Case Style	DG1886 Plastic package, exposed paddle, Lead Finish: Tin-Silver Over Nickel Barrier
Tape & Reel Standard Quantities Available on Reel	F68 7" reels with 20, 50, 100, 200, 500, or 1000 devices 13" reels with 2000, 3000, or 4000 devices
Suggested Layout for PCB Design	PL-838
Evaluation Board	TB-PHA2-13HLNC+ Gerber File
Environmental Ratings	ENV08T1

NOTES

- A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
- B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
- C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the standard terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/terms/viewterm.html

