MMIC DIE

Power Amplifier

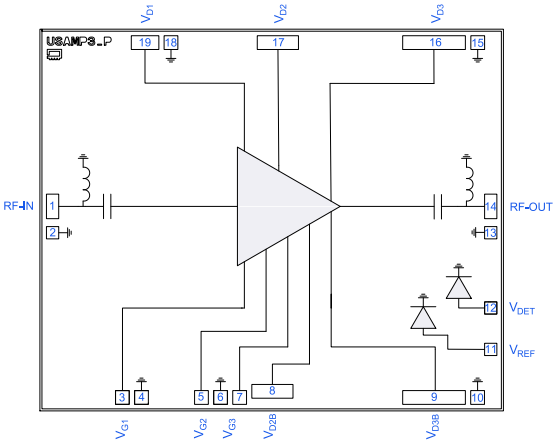
PMA5-123-3W-D+

50Ω 8 to 12 GHz 3.5 W P_{SAT}

THE BIG DEAL

- High Gain, Typ. 29.8 dB
- High P_{SAT}, Typ. +35.5 dBm
- Excellent PAE, Typ. 34.2%
- Supply Voltage, +7 V @ 1250 mA
- Integrated Power Detector

FUNCTIONAL DIAGRAM



SEE ORDERING INFORMATION ON THE LAST PAGE

APPLICATIONS

- Radar, EW, and ECM Defense Systems
- MIMO Wireless Infrastructure Systems
- Microwave Radio & VSAT

PRODUCT OVERVIEW

Mini-Circuits' PMA5-123-3W-D+ is a GaAs MMIC power amplifier operating from 8 to 12 GHz. This internally matched 50Ω amplifier die provides 29.8 dB of gain, +35.5 dBm saturated output power, and +40.2 dBm output IP3, while operating from a +7 V power supply and consuming 1250 mA of current. In addition, an integrated power detector allows for seamless output power monitoring. These characteristics make it ideally suited for microwave radio, satellite communications, and radar systems that require high operating output power, while maintaining very low distortion characteristics.

KEY FEATURES

Features	Advantages
High P_{SAT} Typ. +35.5 dBm	With 3.5 W of output power, this device can be used as a driver stage or as the power amplifier in microwave radio, satellite communications, or radar systems.
High Efficiency PAE Typ. 34.2%	Best-in-class PAE allows for system power conservation and reduced thermal dissipation.
Integrated Power Detector	An on-chip power detector provides a log-linear output voltage over a 0 to +35 dBm output power range. Useful for power monitoring in systems with dynamic gain and output power control.
Unpackaged Die	Bare die component enables integration into hybrid assemblies.

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ELECTRICAL SPECIFICATIONS[1] AT +25°C, V_{DD} = +7 V, UNLESS NOTED OTHERWISE

Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency Range		8		12	GHz
Gain	8		28.3		dB
	9		30.6		
	10		29.8		
	11		29.5		
	12		30.3		
Output Power at 1 dB Compression (P1dB)	8		+34.5		dBm
	9		+35.1		
	10		+35.0		
	11		+34.4		
	12		+34.7		
Output Power at Saturation (P_{SAT})[2]	8		+34.9		dBm
	9		+35.5		
	10		+35.5		
	11		+35.6		
	12		+35.7		
Power Added Efficiency (PAE) at P_{SAT}			34.2		%
Output Third-Order Intercept (P_{OUT} = +20 dBm/Tone)	8		+38.1		dBm
	9		+39.0		
	10		+40.2		
	11		+39.5		
	12		+38.1		
Input Return Loss	8		15		dB
	9		14		
	10		15		
	11		12		
	12		11		
Output Return Loss	8		10		dB
	9		17		
	10		19		
	11		15		
	12		9		
Isolation	8		75		dB
	9		75		
	10		77		
	11		78		
	12		73		
Noise Figure[3]	8		8.6		dB
	9		7.7		
	10		6.9		
	11		6.3		
	12		6.1		
Power Detector Range			0 to +35		dBm
Device Operating Voltage (V_{DD})[4]		+6	+7	+8	V
Device Operating Current (I_{DD})[5]			1250		mA
Device Gate Voltage (V_{GG})[6]			-0.75		V
Device Gate Current (I_{GG})				14	mA
DC Current Variation vs. Temperature[7]			-10		µA/°C
DC Current Variation vs. Voltage[8]			-1.56		µA/mV

1. Tested on Mini-Circuits Die Characterization Test Board. See Figure 3. Loss de-embedded to the RF input and output wire bonds of the device.
2. P_{SAT} is defined as when the Output Power changes 0.1 dB per 1 dB change in Input Power.
3. Noise Figure performance measured on packaged version of amplifier, PMA5-123-3W+.
4. $V_{DD} = V_{D1} = V_{D2} = V_{D3} = V_{D2B} = V_{D3B}$
5. Current at P_{IN} = -10 dBm. Increases to 1450 mA at P1dB.
6. $V_{GG} = V_{G1} = V_{G2} = V_{G3}$
7. (Current at +85°C – Current at -45°C)/(130°C)
8. (Current at +8 V – Current at +6 V)/(+2 V)

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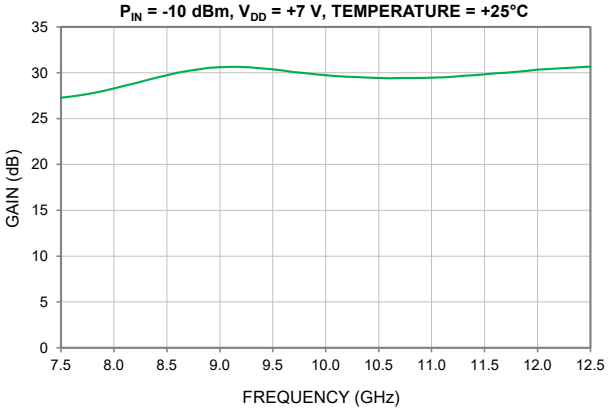
TYPICAL PERFORMANCE GRAPHS

For additional performance graphs, please see the PMA5-123-3W+ datasheet

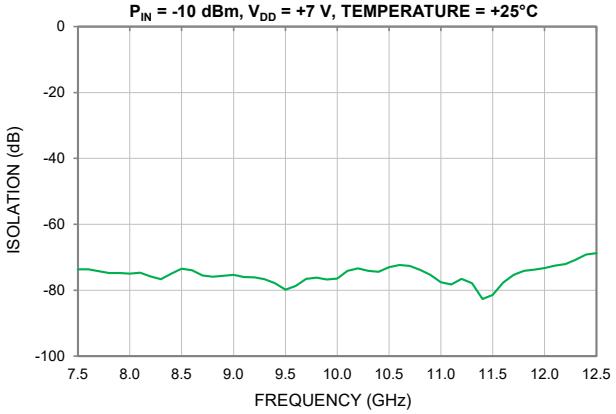
GAIN

P_{IN} = -10 dBm, V_{DD} = +7 V, TEMPERATURE = +25°C



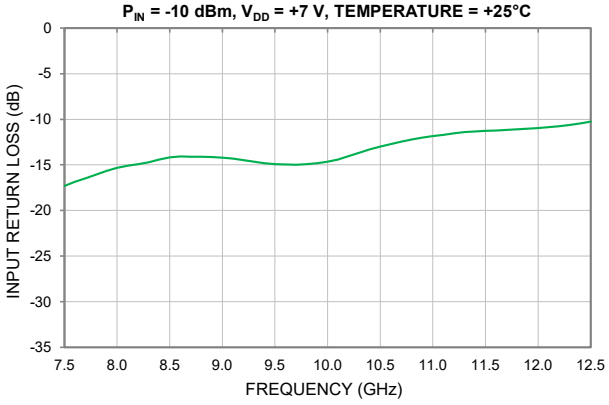
ISOLATION

P_{IN} = -10 dBm, V_{DD} = +7 V, TEMPERATURE = +25°C



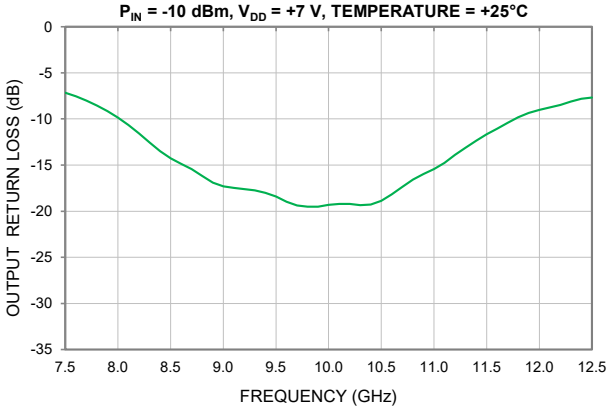
INPUT RETURN LOSS

P_{IN} = -10 dBm, V_{DD} = +7 V, TEMPERATURE = +25°C



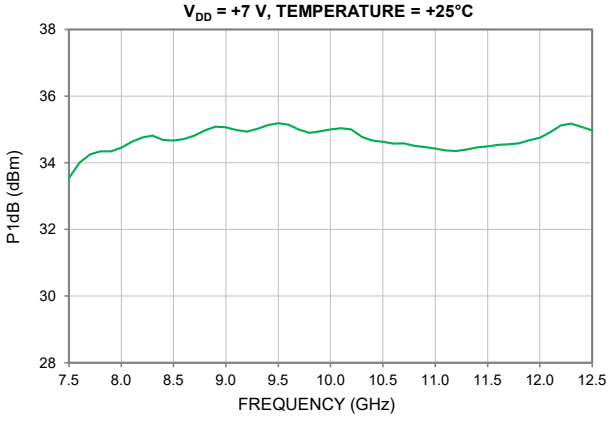
OUTPUT RETURN LOSS

P_{IN} = -10 dBm, V_{DD} = +7 V, TEMPERATURE = +25°C



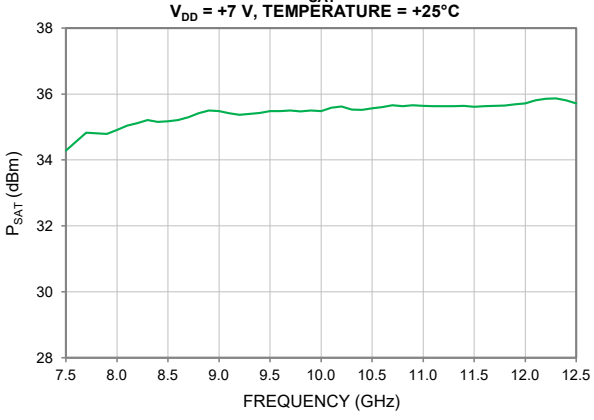
P1dB

V_{DD} = +7 V, TEMPERATURE = +25°C



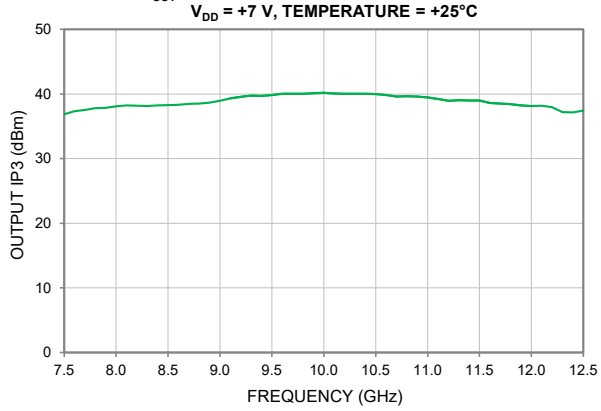
P_{SAT}

V_{DD} = +7 V, TEMPERATURE = +25°C

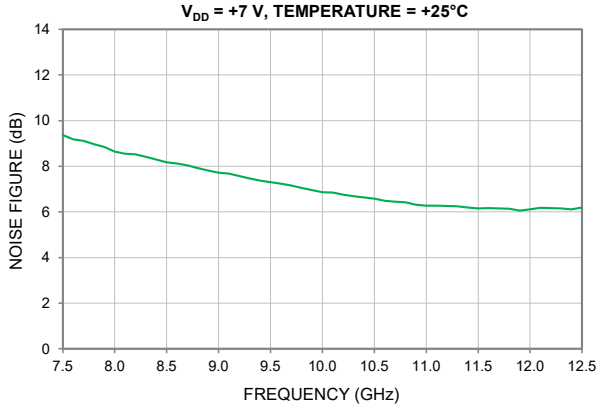


TYPICAL PERFORMANCE GRAPHS

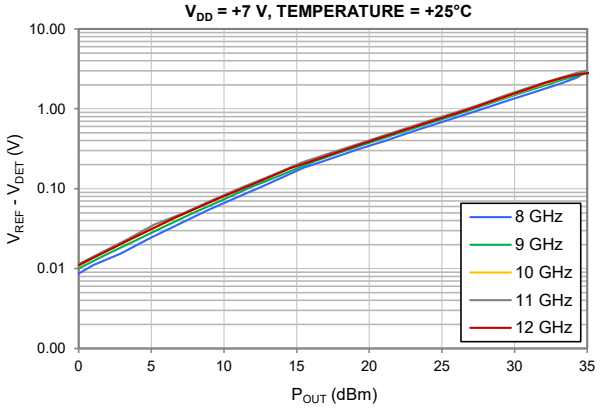
OUTPUT IP3
P_{OUT} = +20 dBm/TONE, TONE SPACING = 5 MHz,
V_{DD} = +7 V, TEMPERATURE = +25°C



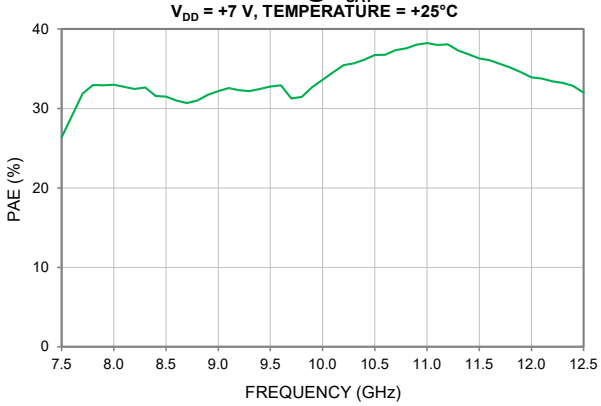
NOISE FIGURE[9]
V_{DD} = +7 V, TEMPERATURE = +25°C



POWER DETECTOR OUTPUT VOLTAGE[10]
V_{DD} = +7 V, TEMPERATURE = +25°C



PAE @ P_{SAT}
V_{DD} = +7 V, TEMPERATURE = +25°C



9. Noise Figure measured on packaged model, PMA5-123-3W+.

10. For more details on Integrated Power Detector please see PMA5-123-3W+ datasheet. Logarithmic scale base 10.

ABSOLUTE MAXIMUM RATINGS[11]

Parameter	Ratings
Operating Temperature[12]	-45°C to +85°C
Storage Temperature (for Die)[13]	-65°C to +150°C
Junction Temperature[14]	+175°C
Total Power Dissipation	14.7 W
Input Power (CW), V_{DD} = +7 V	+27 dBm
DC Drain Voltage at V_{DD}[15]	+8.5 V
DC Gate Voltage at V_{GG}[16]	-3.0 V (min) / -0.4 V (max)
DC Drain Current I_{DD}	3 A
DC Gate Current I_{GG}	14 mA

11. Permanent damage may occur if these limits are exceeded. Maximum ratings are not intended for continuous normal operation.
12. Bottom of Die.
13. For die shipped in Gel-Pack see ENV80 (limited by packaging).
14. Peak temperature on top of Die.
15. $V_{DD} = V_{D1} = V_{D2} = V_{D3} = V_{D2B} = V_{D3B}$
16. $V_{GG} = V_{G1} = V_{G2} = V_{G3}$

THERMAL RESISTANCE

Parameter	Ratings
Thermal Resistance (Θ_{JC})[17]	7.7°C/W

17. Θ_{JC}= (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

ESD RATING[18]

	Class	Voltage Range	Reference Standard
HBM	1B	500 V to < 1000 V	ANSI/ESDA/JEDEC JS-001-2023
CDM	C3	≥ 1000 V	ANSI/ESDA/JEDEC JS-002-2022

ESD HANDLING PRECAUTION: This device is designed to be Class 1B for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage.

18. Tested in 5x5 mm 32-Lead QFN-Style Package.

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FUNCTIONAL DIAGRAM

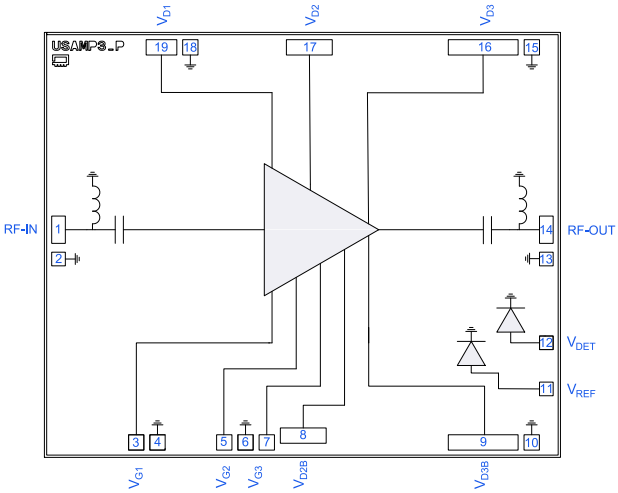

Figure 1. PMA5-123-3W-D+ Functional Diagram

PAD DESCRIPTION

Function	Pad Number	Description (Refer to Figure 1)
RF-IN	1	RF-IN pad connects to RF Input port.
RF-OUT	14	RF-OUT pad connects to RF Output port.
V_{D1}	19	DC Input pad connects to First Stage Drain Voltage port.
V_{G1}	3	DC Input pad connects to First Stage Gate Voltage port.
V_{D2}	17	DC Input pad connects to Second Stage Drain Voltage port.
V_{G2}	5	DC Input pad connects to Second Stage Gate Voltage port.
V_{D3}	16	DC Input pad connects to Third Stage Drain Voltage port.
V_{G3}	7	DC Input pad connects to Third Stage Gate Voltage port.
V_{D2B}[18]	8	DC Input pad connects to Second Stage Drain Voltage Alternate port.
V_{D3B}[19]	9	DC Input pad connects to Third Stage Drain Voltage Alternate port.
V_{DET}	12	DC Output pad connects to Power Detector Output Voltage port. Voltage is proportional to RF Output Power.
V_{REF}	11	DC Input pad connects to Power Detector Reference Voltage port.
GND	2, 4, 6, 10, 13, 15, 18, & Bottom of Die	Connects to die backside through vias. Bond wires to ground are optional.

18. V_{D2B} can be used as an alternate to V_{D2}. V_{D2B} and V_{D2} are connected internally. Voltage may be applied to both ports.
19. V_{D3B} can be used as an alternate to V_{D3}. V_{D3B} and V_{D3} are connected internally. For optimal performance voltage should be applied to both ports. During characterization, V_{D3} and V_{D3B} were connected via a jumper.

DIE OUTLINE: inches [mm], Typical

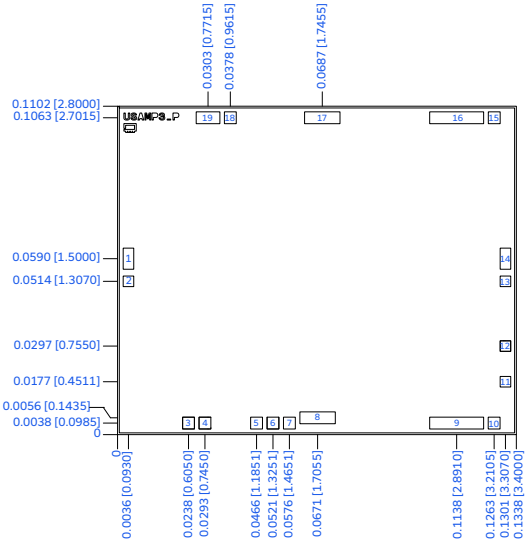

Figure 2. PMA5-123-3W-D+ Die Outline

DIMENSIONS: inches [mm], Typical

Die Size	0.1338 x 0.1102 [3.4000 x 2.8000]
Die Thickness	0.0039 [0.1000]
Bond Pad Sizes:	
Pads 1, 14	0.0035 x 0.0070 [0.0900 x 0.1800]
Pads 2, 11, 12, 13	0.0035 x 0.0035 [0.0900 x 0.0900]
Pads 3, 4, 5, 6, 7, 10, 15, 18	0.0039 x 0.0039 [0.1010 x 0.1010]
Pads 8, 17	0.0119 x 0.0039 [0.3020 x 0.1010]
Pads 9, 16	0.0181 x 0.0039 [0.4600 x 0.1010]
Pad 19	0.0079 x 0.0039 [0.2020 x 0.1010]
Plating (Pads & Bottom of Die)	Gold

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CHARACTERIZATION BOARD

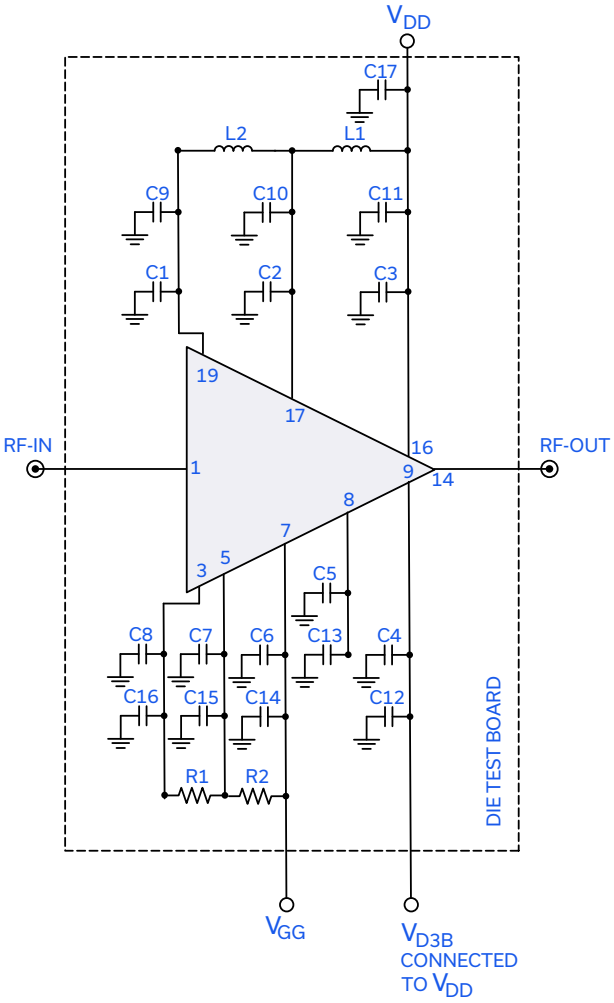

Figure 3. PMA5-123-3W-D+ Characterization Circuit

Electrical Parameters and Conditions
Gain, Return Loss, Output Power at 1 dB Compression (P1dB), Output IP3 (OIP3), and Noise Figure measured using N5247B PNA-X Microwave Network Analyzer.

Conditions:
a. Gain and Return Loss: P_{IN} = -10 dBm
b. Output IP3 (OIP3): Two tones, spaced 5 MHz apart, +20 dBm/tone at output.

Power ON/Power OFF Sequence
Caution: Permanent damage to the device will occur if the Power ON and Power OFF sequence are not followed

POWER ON:
1) Set V_{GG} = -1.5 V. Apply V_{GG}.
2) Set V_{DD} = +7 V. Apply V_{DD}.
3) Increase V_{GG} to obtain desired I_{DD} as shown in spec table.
4) Apply RF Signal.

POWER OFF:
1) Turn off RF Signal.
2) Adjust V_{GG} down to -1.5 V.
3) Turn off V_{DD}.
4) Turn off V_{GG}.

Component	Value	Size	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8	1000 pF	0402	GRM1555C1H102JA01D	MURATA
C9, C10, C11, C12, C13, C14, C15, C16	0.1 µF	0402	GRM155R71E104KE14D	MURATA
L1, L2	150 nH	0402	0402DF-151XJRW	COILCRAFT
R1	100Ω	0402	RK73H1ETTP1000F	KOA SPEER
R2	0Ω	0402	RK73Z1ETTP	KOA SPEER
C17	47 µF	1206	1206YD476MAT2A	KYOCERA AVX

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ASSEMBLY DIAGRAM

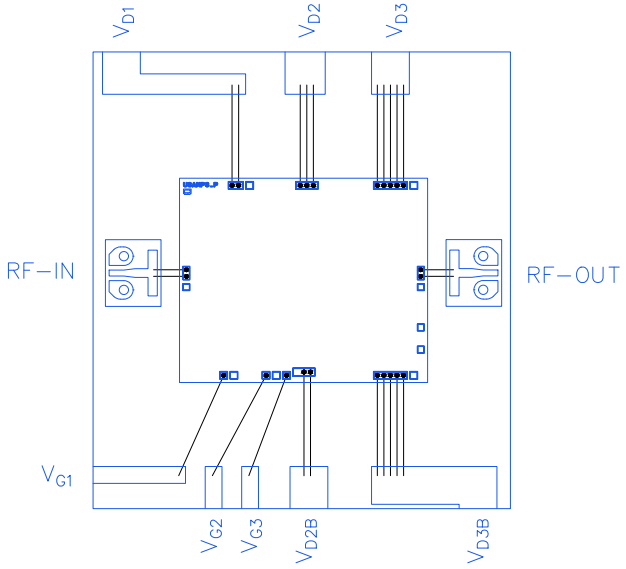

Figure 4. PMA5-123-3W-D+ Assembly Diagram

- Bond wire diameter: 1 mil
- Bond wire height: 5 mils
- Typical gap from Die edge to launcher edge: 5 mils
- Capacitive Stub dimensions: 25 mils by 5 mils Alumina substrates.
- PCB thickness and material: 8 mil RO4003C (Thickness: 1 oz copper on each side).

ASSEMBLY AND HANDLING PROCEDURE

1. Storage
   Die should be stored in a dry nitrogen purged desiccator or equivalent.
2. ESD Precautions
   MMIC pHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in anti-static protected material, which should be opened only in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
   Devices require careful handling using tools appropriate for manipulating semiconductor chips. It is recommended to handle the chips along the edges with a custom designed collet. The surface of the chips should not be touched with a vacuum collet, tweezers, or fingers. The die mounting surface must be clean and flat. Using conductive silver-filled epoxy, apply sufficient adhesive to meet the required bond line thickness, fillet height and coverage around the total periphery of the device. The recommended epoxy is ATROX 800HT5 or equivalent. Parts should be cured in a nitrogen-filled atmosphere per manufacturer's recommended cure profile.
4. Wire Bonding
   Openings in the surface passivation above the gold bond pads are provided to allow wire bonding to the die. Thermosonic bonding is recommended with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. The suggested interconnect is pure gold, 1 mil diameter wire. Bonds are recommended to be made from the bond pads on the die to the package or substrate. All bond wire length and bond wire height should be kept as short as possible, unless specified by design, to minimize performance degradation due to undesirable series inductance

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ADDITIONAL DETAILED INFORMATION IS AVAILABLE ON OUR DASHBOARD CLICK HERE

Performance Data	Table Graphs S-Parameter (S2P Files) Data Set (.zip file)	
Case Style	Die	
RoHS Status	Compliant	
Die Ordering and Packaging Information	Quantity, Package	Model No.
	Gel - Pak: 5, 10, or 50 KGD*	PMA5-123-3W-DG+
	Medium†, Partial wafer: KGD*<270	PMA5-123-3W-DP+
	Full wafer†	PMA5-123-3W-DF+
	†Available upon request contact sales representative. Refer to AN-60-067	
Die Marking	USAMP3_P	
Environmental Ratings	ENV80	

* Known Good Die ("KGD") means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within a predefined range. While DC testing is not definitive, it does provide a high degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuits' applicable established test performance criteria and measurement instructions.

C. The parts covered by this specification document are subject to Mini-Circuits' standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/terms/viewterm.html

D. Mini-Circuits does not warrant the accuracy or completeness of the information, text, graphics and other items contained within this document and same are provided as an accommodation and on an as is basis, with all faults.

E. Purchasers of this part are solely responsible for proper storing, handling, assembly and processing of known good die (KGD) (including, without limitation, proper ESD preventative measures, die preparation, die attach, wire bonding and related assembly and test activities), and Mini-Circuits assumes no responsibility therefor or for environmental effects on KGD.