MMIC DIE

Power Amplifier

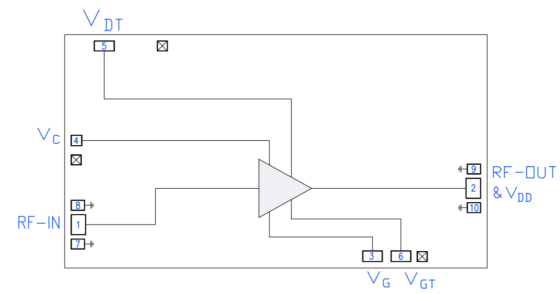
PMA5-223-D+

50Ω 0.01 to 22 GHz Wideband Amplifier

THE BIG DEAL

- Wide Bandwidth 10 MHz to 22 GHz
- P_{SAT}, Typ. +33.5 dBm
- Linear Gain, Typ. 16 dB
- IM3, Typ. -42 dBc @ P_{OUT} = +20 dBm/tone
- Supply Voltage, +15 V at 500 mA

FUNCTIONAL DIAGRAM



SEE ORDERING INFORMATION ON THE LAST PAGE

APPLICATIONS

- Test and Measurement Equipment
- 5G MIMO and Backhaul Radio
- Satellite Communication
- Radar, EW, and ECM Defense Systems

PRODUCT OVERVIEW

The PMA5-223-D+ is a GaAs pHEMT MMIC power amplifier operating from 0.01 to 22 GHz. The wideband distributed amplifier provides 16 dB of linear gain, +33.5 dBm saturated output power, and achieves +41 dBm output IP3 at 10 GHz. The device operates from a +15 V supply and consumes 500 mA of quiescent current. The amplifier is 50Ω matched at the input and output, making it easy to implement. These characteristics make it ideally suited for wideband test instrumentation, satellite communications, and defense systems that require high operating output power while maintaining very low distortion characteristics.

KEY FEATURES

Features	Advantages
Gain, Typ. 16 dB P_{SAT}, Typ. +33.5 dBm	Flat, broadband gain and high output power without high frequency roll-off make this device excellent for wide-band systems from 0.01 to 22 GHz that require at least 1 W of operating output power over the full band.
At P_{OUT} = +20 dBm/tone: • OIP2, Typ. +43 dBm • OIP3, Typ. +41 dBm	High operating OIP2 and OIP3 provide low in-band IM distortion products, enabling minimal signal-to-noise degradation in high fidelity measurement and communication systems.
Wide Bandwidth: 10 MHz to 22 GHz	Supports a variety of broadband and narrowband applications without the need to reconfigure circuitry.
Unpackaged Die	Suitable for chip and wire hybrid assemblies. This device is matched to 50Ω at the input and output and measures only 3.27×1.81 mm.

REV. A
ECO-030312
PMA5-223-D+
MCL NY
260706

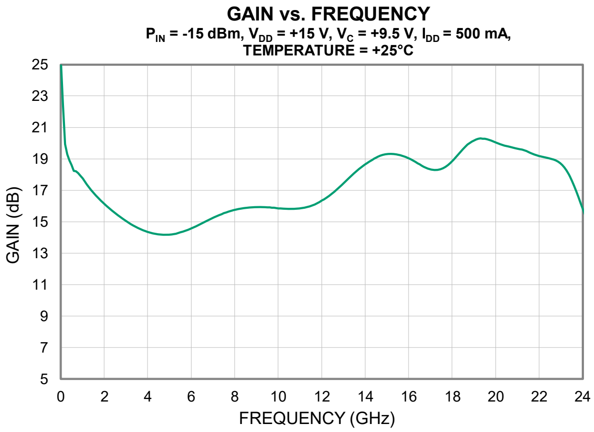
ELECTRICAL SPECIFICATIONS[1] AT +25 °C, V_{DD} = +15 V, UNLESS NOTED OTHERWISE

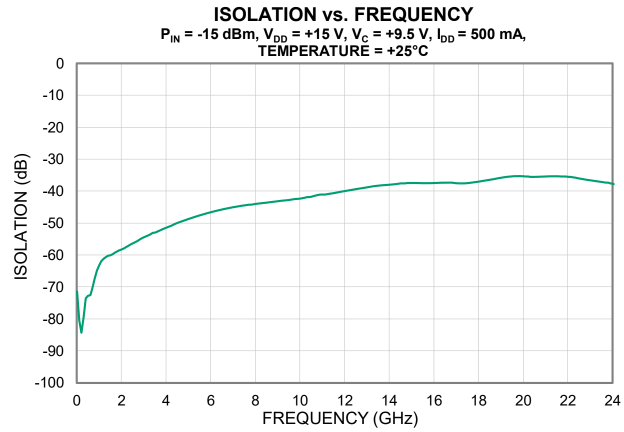
Parameter	Frequency (GHz)	Min.	Typ.	Max.	Units
Frequency Range		0.01		22	GHz
Gain	0.1 1 5 10 15 22	19.3 15.7 12.4 13.4 16.2 13.7	22.5 17.7 14.1 16.0 19.1 18.9		dB
Input Return Loss	0.1 1 5 10 15 22		40 18 13 12 17 7		dB
Output Return Loss	0.1 1 5 10 15 22		21 13 9 10 14 10		dB
Isolation	0.1–22		44		dB
Output Power at 1 dB Compression (P1dB)	0.1 1 5 10 15 22		+27.8 +30.2 +31.4 +31.3 +29.8 +26.8		dBm
Output Power at Saturation (P_{SAT})[2]	0.1 1 5 10 15 22		+34.1 +34.5 +34.7 +33.5 +32.8 +30.5		dBm
Output Third-Order Intercept (P_{OUT} = +20 dBm)	0.1 1 5 10 15 22		+38.3 +39.1 +41.4 +41.2 +41.8 +38.2		dBm
2nd Harmonic (P_{OUT} = + 20 dBm)	0.1 1 5 10 15 22		-39.1 -40.7 -29.6 -27.8 -27.7 -35.8		dBc
Noise Figure	1 5 10 15 22		6.7 3.1 2.4 2.9 5.2		dB
Device Operating Voltage (V_{DD})			+15		V
Device Operating Current (I_{DD})[3]			500		mA
Control Voltage (V_C)			+9.5		V
Gate Voltage (V_G)			-0.5		V
Device Gate Current on V_G (I_G)			2.94		µA
Device Control Current on V_C (I_C)			402		µA
DC Current Variation vs. Temperature			167.87		µA/°C
DC Current Variation vs. Voltage			0.93		µA/mV

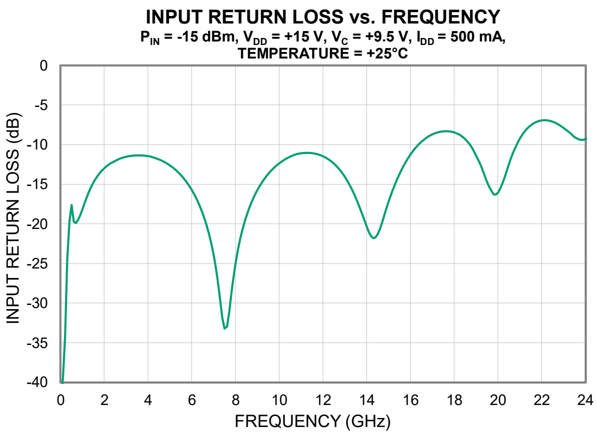
1. Tested on Mini-Circuits Die Characterization Test Board. See Figure 3. Board loss de-embedded to the device.
2. P_{SAT} is defined as when the output power changes 0.1 dB per 1 dB change in input power.
3. Current at P_{IN} = -15 dBm. Increases to 585 mA at P1dB.

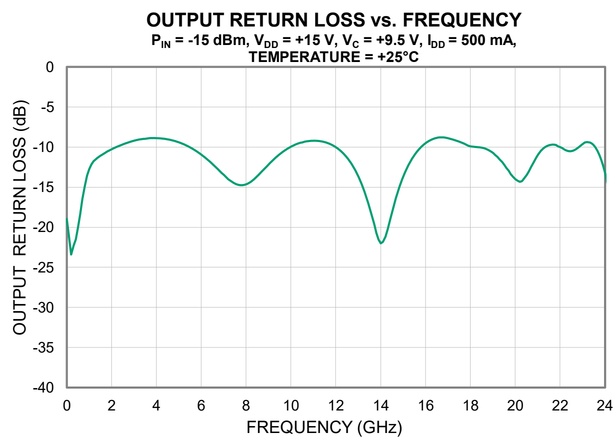
TYPICAL PERFORMANCE GRAPHS

Note: The following data was taken on a Mini-Circuits DIE Characterization Test Board with external bias tee. All data taken at nominal condition of V_{DD} = +15 V, V_C = +9.5 V, V_G was adjusted at each voltage and temperature level to achieve I_{DD} = 500 mA. For over temperature and expanded bias point data, see PMA5-223+.









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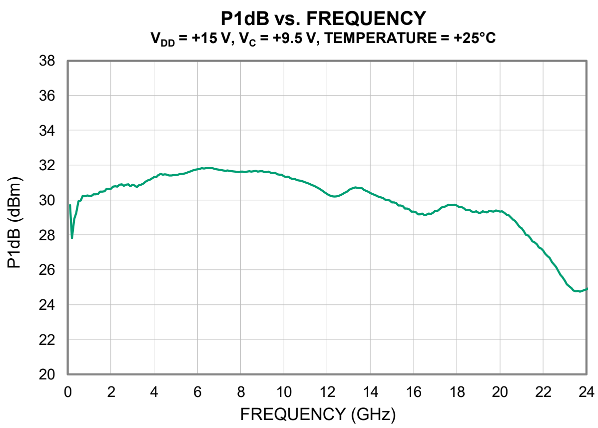

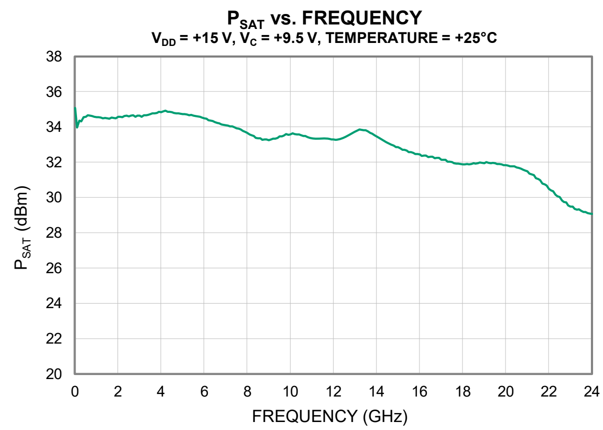

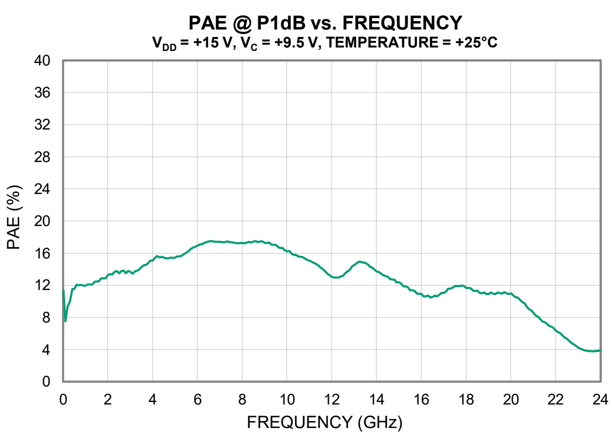

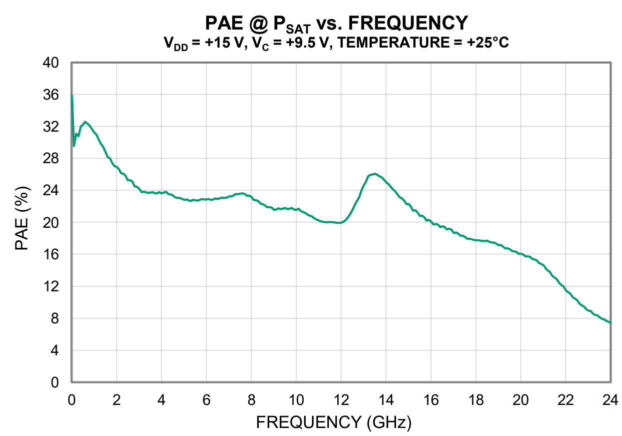

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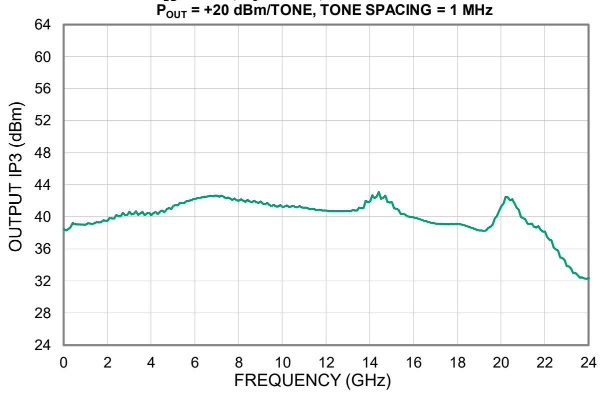
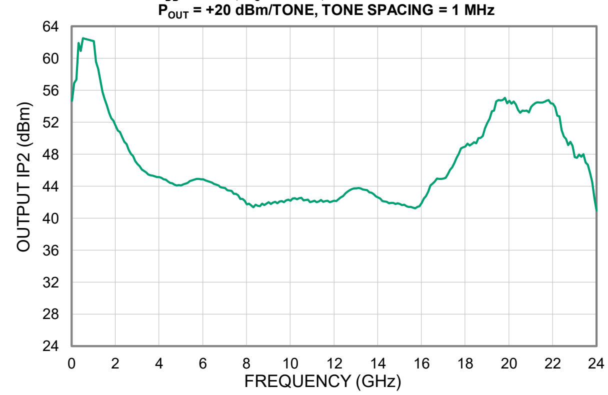
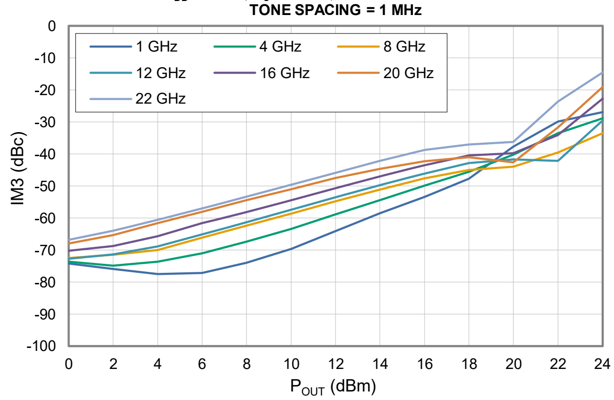
OUTPUT IP3 vs. FREQUENCY
V_{DD} = +15 V, V_C = +9.5 V, TEMPERATURE = +25°C
P_{OUT} = +20 dBm/TONE, TONE SPACING = 1 MHz



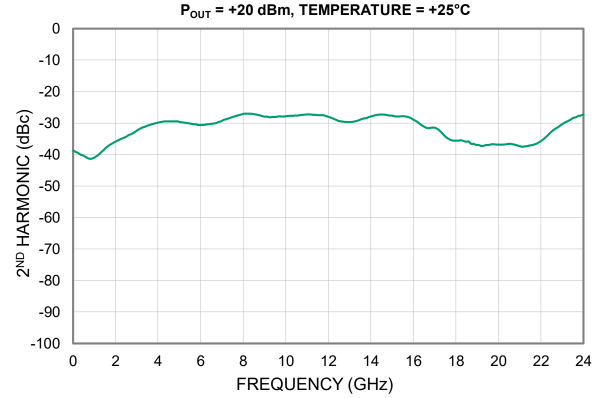
OUTPUT IP2 vs. FREQUENCY
V_{DD} = +15 V, V_C = +9.5 V, TEMPERATURE = +25°C
P_{OUT} = +20 dBm/TONE, TONE SPACING = 1 MHz



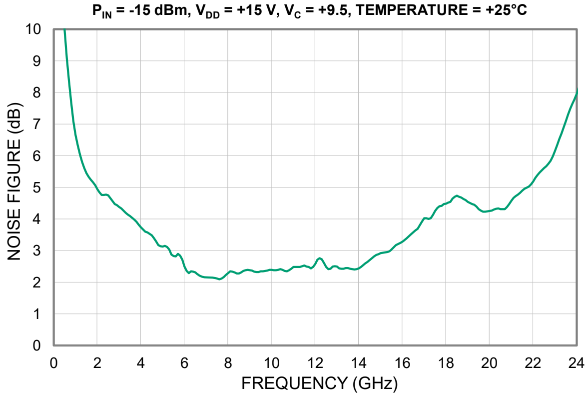
IM3 vs. P_{OUT}/TONE
V_{DD} = +15 V, V_C = +9.5 V, TEMPERATURE = +25°C
TONE SPACING = 1 MHz



2ND HARMONIC vs. FREQUENCY
P_{OUT} = +20 dBm, TEMPERATURE = +25°C



NOISE FIGURE vs. FREQUENCY
P_{IN} = -15 dBm, V_{DD} = +15 V, V_C = +9.5, TEMPERATURE = +25°C



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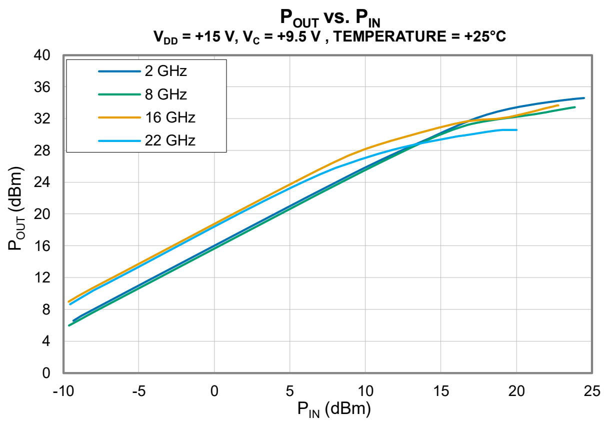

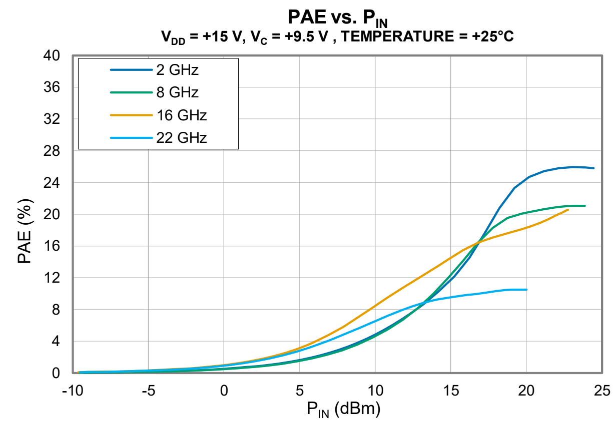

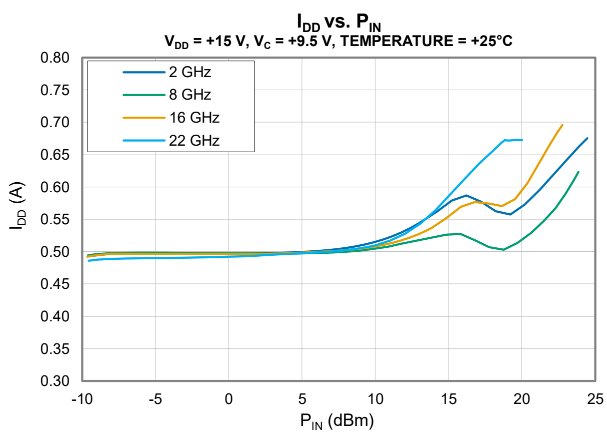

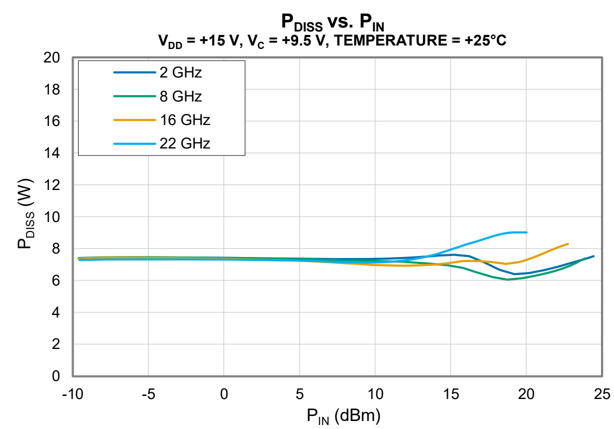

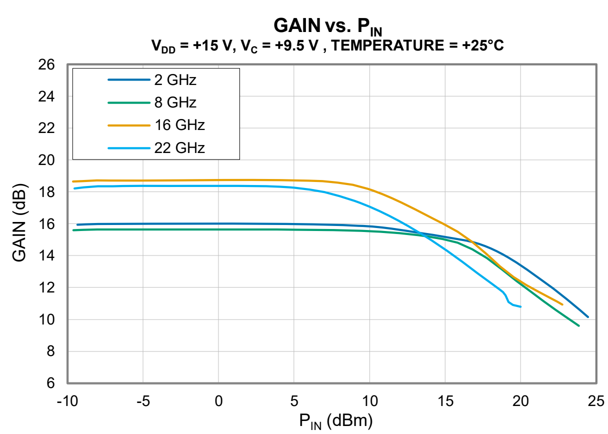

ABSOLUTE MAXIMUM RATINGS[4]

Parameter	Ratings
Operating Temperature	-40 °C to +85 °C
Storage Temperature	-65 °C to +150 °C
Junction Temperature[5]	+175°C
Total Power Dissipation	11 W
Input Power (CW), V_{DD} = +15 V	+27 dBm
DC Drain Voltage at RF-OUT & V_{DD}	+16 V
DC Gate Voltage at V_G	-0.25 V
DC Control Voltage at V_C	+10.3
DC Drain Current I_{DD}	800 mA
DC Gate Current I_G	0.6 mA
DC Control Current I_C	8.2 mA

4. Permanent damage may occur if any of these limits are exceeded. Maximum ratings are not intended for continuous normal operation.
5. Peak Temperature on top of Die.

THERMAL RESISTANCE

Parameter	Ratings
Thermal Resistance (Θ_{JC})[6]	8.2 °C/W

6. Θ_{JC}= (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

ESD RATING[7]

	Class	Voltage Range	Reference Standard
HBM	1B	500 to < 750	ANSI/ESDA/JEDEC JS-001-2023
CDM	C3	≥ 1000	ANSI/ESDA/JEDEC JS-002-2025

7. ESD measured in a 5x5 mm 32-Lead QFN-Style package.

ESD HANDLING PRECAUTION: This device is designed to be Class 1B for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage.

FUNCTIONAL DIAGRAM

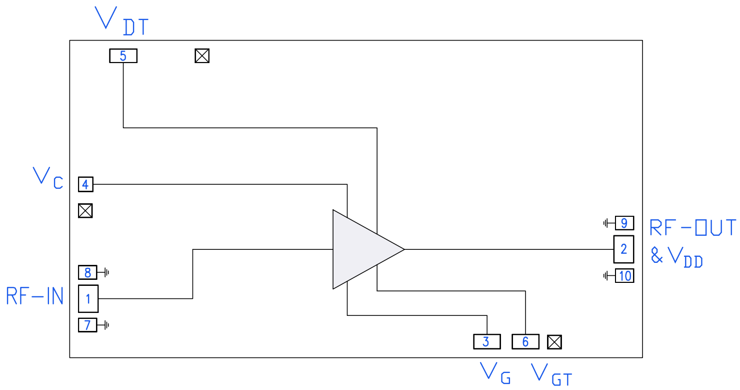

Figure 1. PMA5-223-D+ Functional Diagram

PAD DESCRIPTION

Function	Pad Number	Description (Refer to Figure 3)
RF-IN[8]	1	RF-IN Pad connects to RF Input port.
RF-OUT & V_{DD}[9]	2	RF-OUT pad connects to RF-Output port.
V_G	3	DC Input pads connect to voltage input ports, V_G.
V_C	4	DC Input pads connect to control voltage ports, V_C.
V_{DT}	5	DC Input pads connect to input ports for drain termination, V_{DT}.
V_{GT}	6	DC Input pads connect to input ports for gate termination, V_{GT}.
GND	7-10, & Bottom of Die	Connected to die backside through vias. Bond wires to ground are optional.

8. DC Blocking Capacitor is required.
9. External Bias-Tee is required.

DIE OUTLINE: inches [mm], Typical

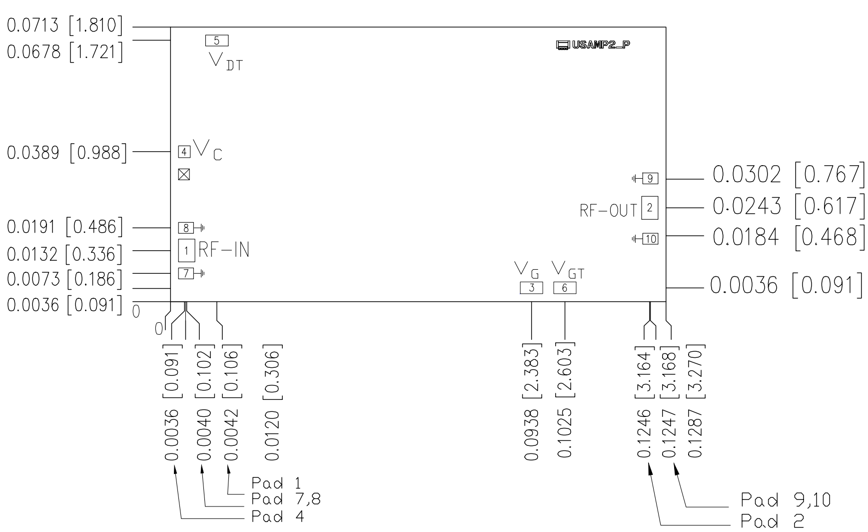

Figure 2. PMA5-223-D+ Die Outline

DIMENSIONS: inches [mm], Typical

Die Size	0.1287 x 0.0713 [3.27 x 1.81]
Die Thickness	0.0040 [0.100]
Bond Pad Sizes:	
Pad 1-2	0.0043 x 0.0059 [0.109 x 0.151]
Pad 3-6	0.0058 x 0.0031 [0.148 x 0.078]
Pad 4	0.0031 x 0.0031 [0.078 x 0.078]
Pad 5	0.0059 x 0.0029 [0.151 x 0.073]
Pad 7-10	0.0039 x 0.0029 [0.100 x 0.073]
Plating (Pads & Bottom of Die)	Gold

CHARACTERIZATION TEST BOARD

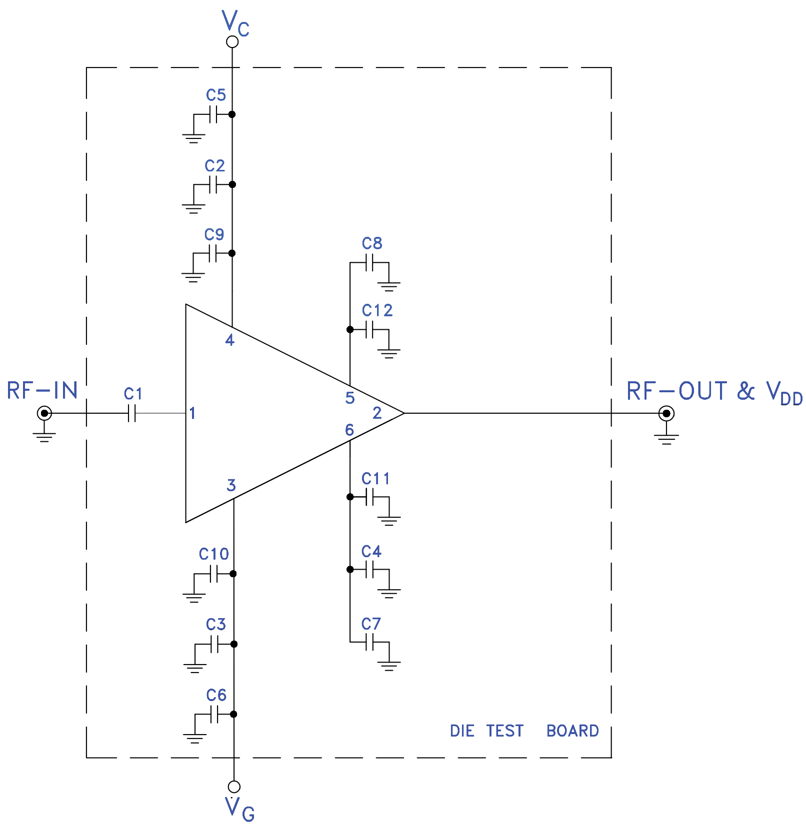

Figure 3. PMA5-223-D+ Characterization and Application Circuit

Electrical Parameters and Conditions
Gain, Return Loss, Output Power at 1dB Compression (P1dB), Output IP3 (OIP3), Output Power at Saturation (P_{SAT}), and Noise Figure measured using PNA-X N5245B Microwave Network Analyzer.

Conditions:
1. Gain and Return Loss: P_{IN} = -15 dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, +20 dBm/Tone at output.
3. V_{DD} = +15 V, V_C = +9.5 V
4. Typical Gate Voltage required is around -0.5 V to achieve I_{DD} = 0.5 A.

Power ON/Power OFF Sequence Caution: Permanent damage to the device will occur if the Power ON and Power OFF sequences are not followed.

POWER ON:
1) Ensure V_G, V_C and V_{DD} are OFF.
2) Set V_G = -1.5 V. Apply V_G.
3) Set V_C = +9.5 V. Apply V_C.
4) Set V_{DD} = +15 V. Apply V_{DD}.
5) Increase V_G to obtain the desired I_{DD} as shown in specification table.
6) Apply RF Signal.

POWER OFF:
1) Turn off RF Signal.
2) Adjust V_G to -1.5 V.
3) Turn off V_{DD}.
4) Turn off V_C.
5) Turn off V_G.

Component	Value	Size	Part Number	Manufacturer
C1	0.1 µF	0201	0201BB104KW160	PASSIVE PLUS
C2-C4	0.1 µF	0402	GRM155R71E104KE14D	MURATA
C5-C8	1 µF	0603	06035C105KAT2A	AVX CORP.
C9-C12	100 pF	0.022×0.022 IN	MA4M3100	MACOM

ASSEMBLY DIAGRAM

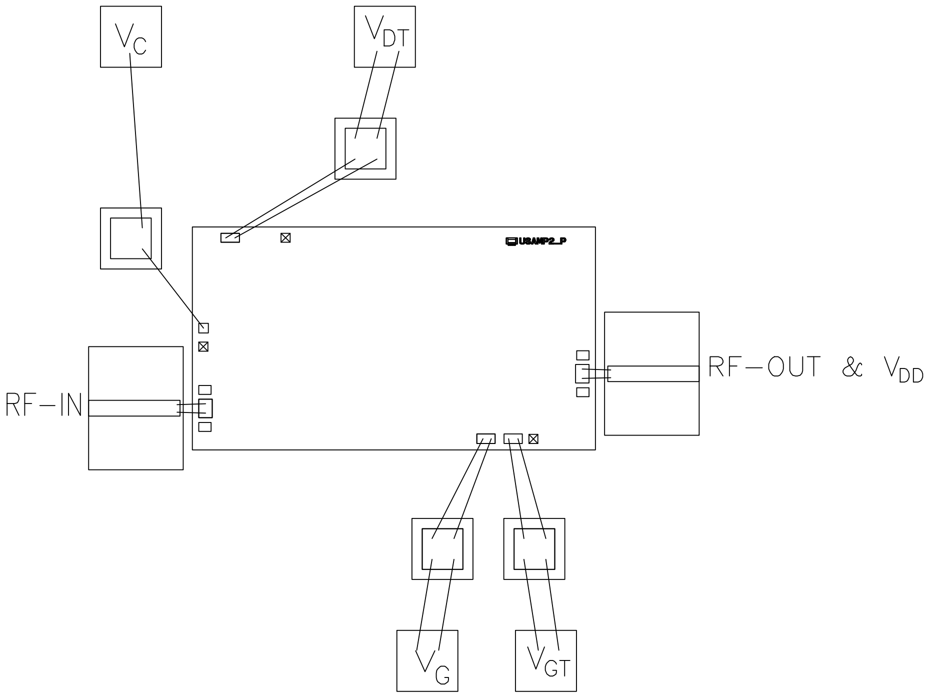

Figure 4. PMA5-223-D+ Assembly Diagram

- Bond wire diameter: 1 mil
- Bond wire lengths from die pad to PCB at RF-IN and RF-OUT: 9 mil ± 2 mils
- Bond wire length from die pad to capacitor near V_{DT}: 50 mil ± 2 mils
- Bond wire length from die pad to capacitor near V_{C}: 32 mil ± 2 mils
- Bond wire length from die pad to capacitor near V_{G}: 36 mil ± 2 mils
- Bond wire length from die pad to capacitor near V_{GT}: 32 mil ± 2 mils
- Typical gap from die edge to PCB edge: 3 mils

ASSEMBLY AND HANDLING PROCEDURE

1. Storage
   Die should be stored in a dry nitrogen purged desiccator or equivalent.
2.  ESD Precautions
   MMIC pHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in anti-static protected material, which should be opened only in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
   Devices require careful handling using tools appropriate for manipulating semi conductor chips. It is recommended to handle the chips along the edges with a custom designed collet. The surface of the chips have exposed air bridges and should not be touched with a vacuum collet, tweezers or fingers. The die mounting surface must be clean and flat. Using conductive silver-filled epoxy, apply sufficient adhesive to meet the required bond line thickness, fillet height and coverage around the total periphery of the device. The recommended epoxy is Atrox 800HT5 or equivalent. Parts should be cured in a nitrogen-filled atmosphere per manufacturer's recommended cure profile.
4. Wire Bonding Openings in the surface passivation above the gold bond pads are provided to allow wire bonding to the die. Thermosonic bonding is recommended with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. The suggested interconnect is pure gold, 1 mil diameter wire. Bonds are recommended to be made from the bond pads on the die to the package or substrate. All bond wire length and bond wire height should be kept as short as possible, unless specified by design, to minimize performance degradation due to undesirable series inductance.

ADDITIONAL DETAILED INFORMATION IS AVAILABLE ON OUR DASH BOARD CLICK HERE

Performance Data & Graphs	Data Graphs S-Parameter (S2P Files) Data Set (.zip file)	
Case Style	Die	
RoHS Status	Compliant	
Die Ordering and Packaging Information	Quantity, Package	Model No.
	Gel - Pak: 5,10,50 KGD*	PMA5-223-DG+
	Medium†, Partial wafer: KGD*<288	PMA5-223-DP+
	Full wafer†	PMA5-223-DF+
	†Available upon request contact sales representative. Refer to AN-60-067	
Die Marking	USAMP2_P	
Environmental Ratings	ENV80	

* Known Good Die ("KGD") means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within a predefined range. While DC testing is not definitive, it does provide a higher degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuits' applicable established test performance criteria and measurement instructions.

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